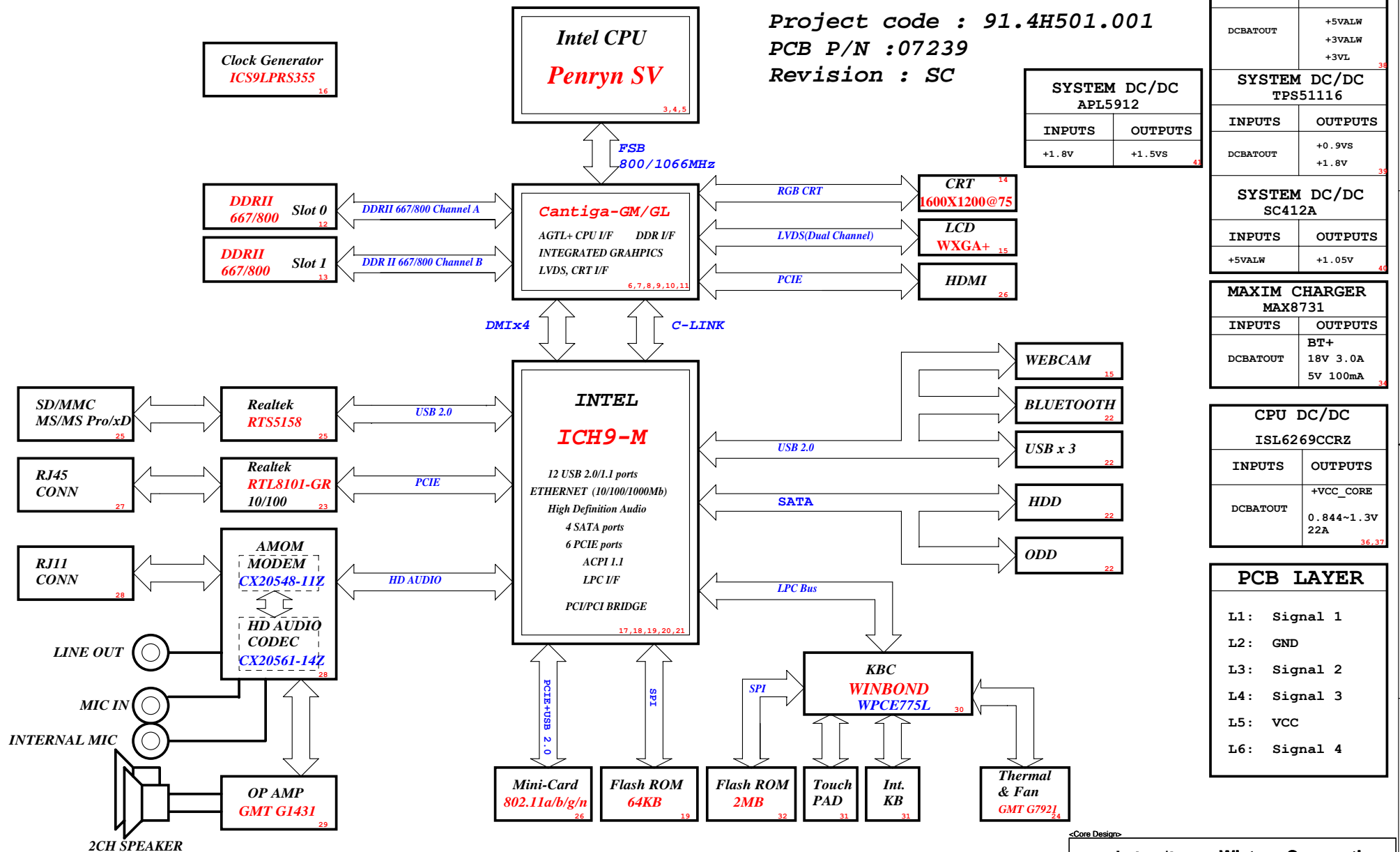


Warrior Intel UMA Block Diagram



ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

PCIE Routing

page 19

LANE1	LAN
LANE2	MiniCard WLAN

USB Table

page 19

Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

SMBus

KBC

ICH9M

Thermal

BATTERY

MINI

Clock Generator

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIOD20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG6 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality(Default)
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in Order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) 11 = Disabled (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Table of Content

Warrior

SC

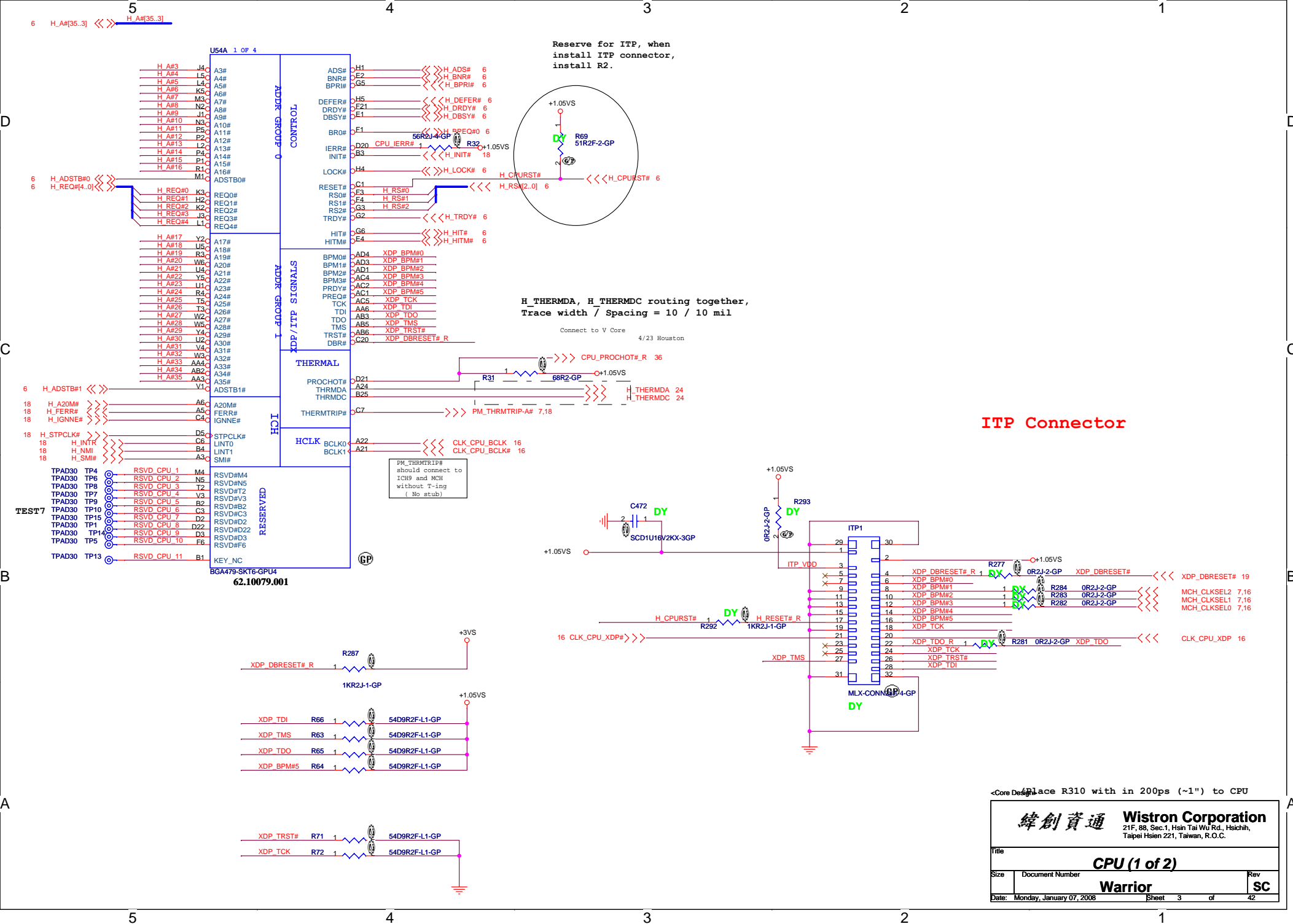
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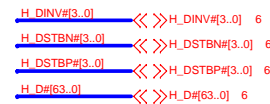
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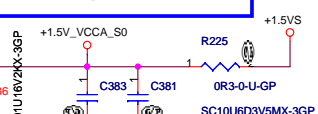
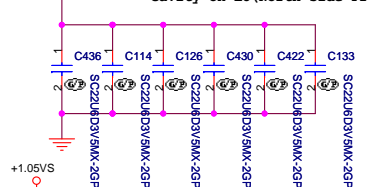
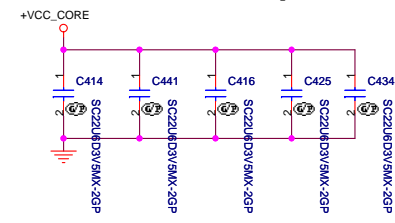
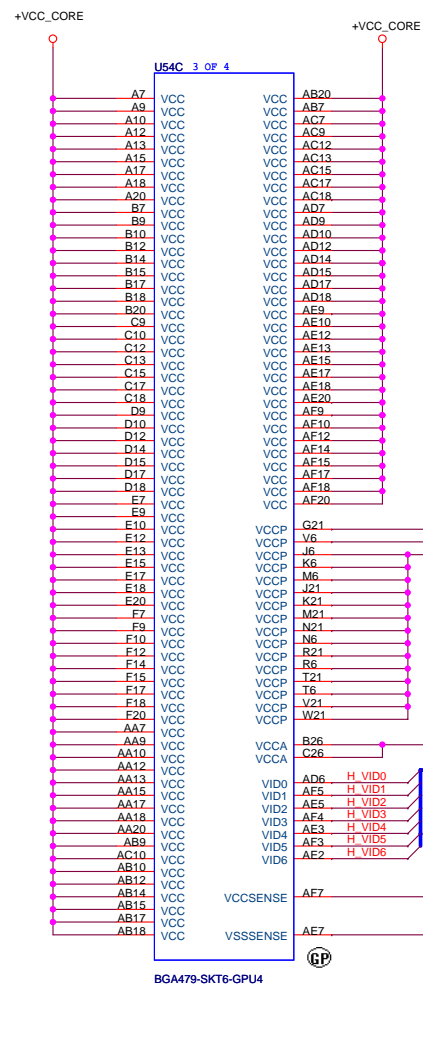
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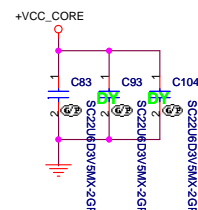
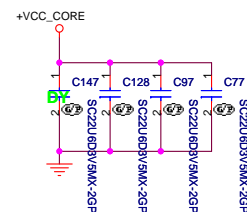
Layout Note:
Comp0, 2 connect with $Z_0=27.4$ ohm, make
trace length shorter than $0.5''$.
Comp1, 3 connect with $Z_0=55$ ohm, make
trace length shorter than $0.5''$.



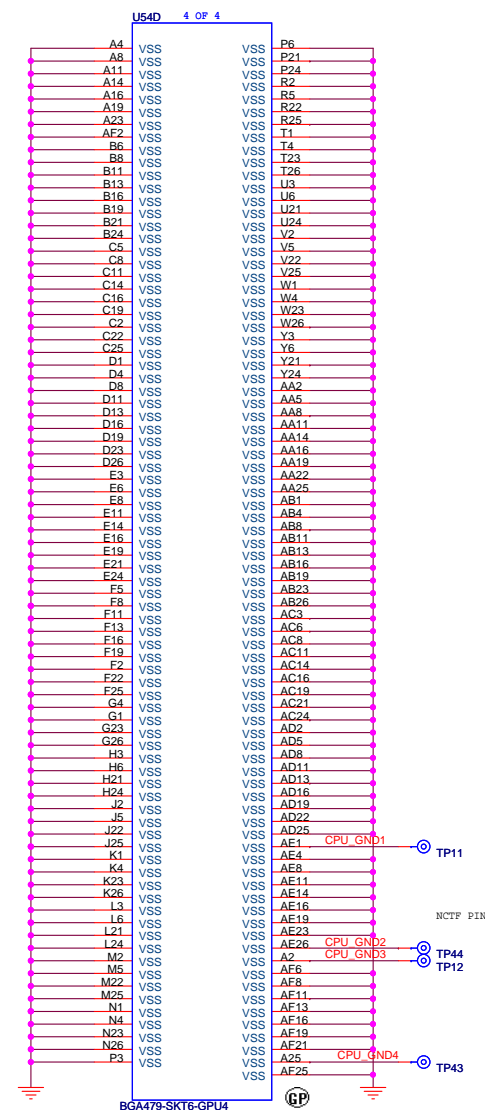
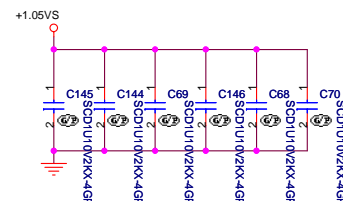
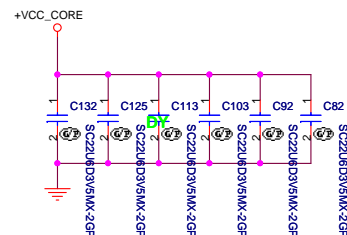
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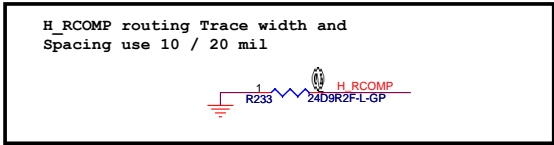
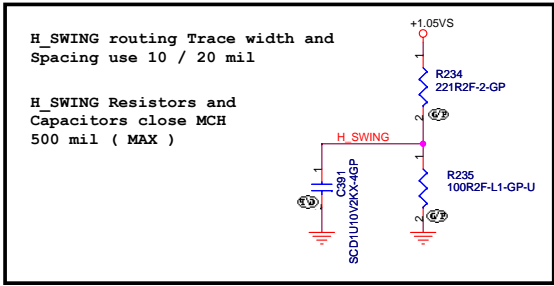
VCCSENSE and VSSSENSE lines should be of equal length.

Please these inside socket
cavity on L8 (North side Secondary)

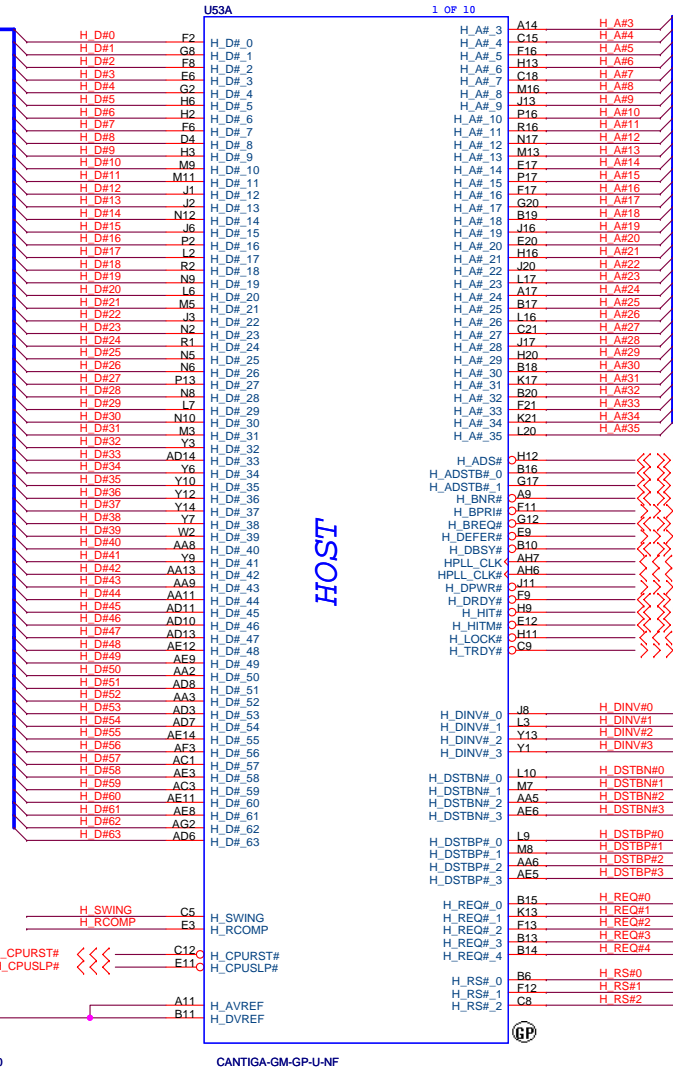
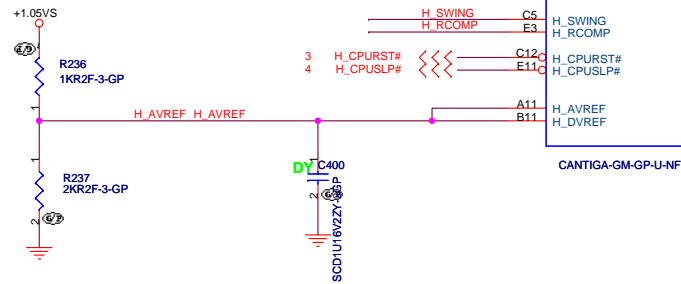


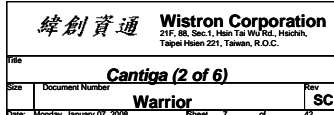
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cavity on L8 (South side Primary)

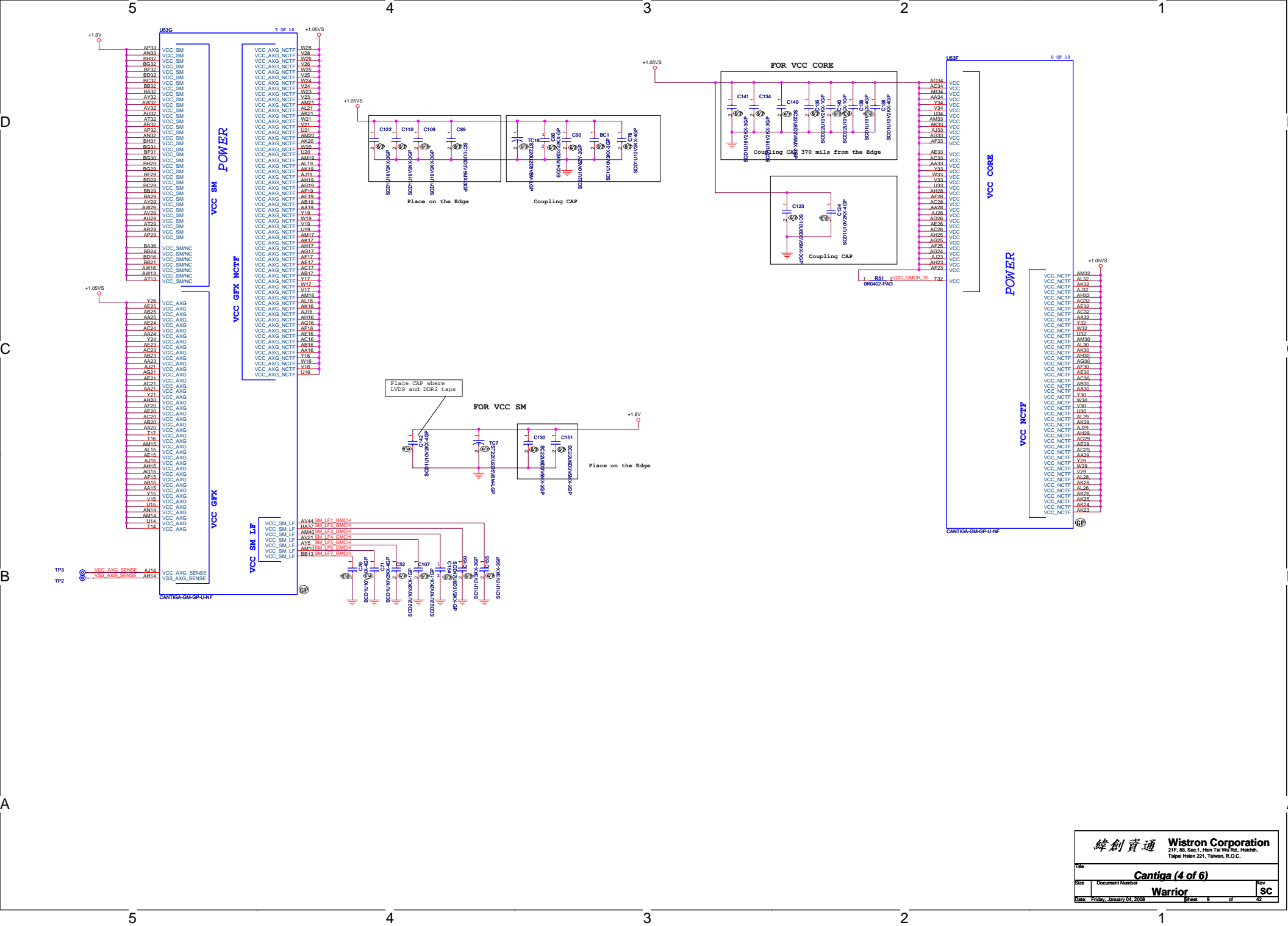




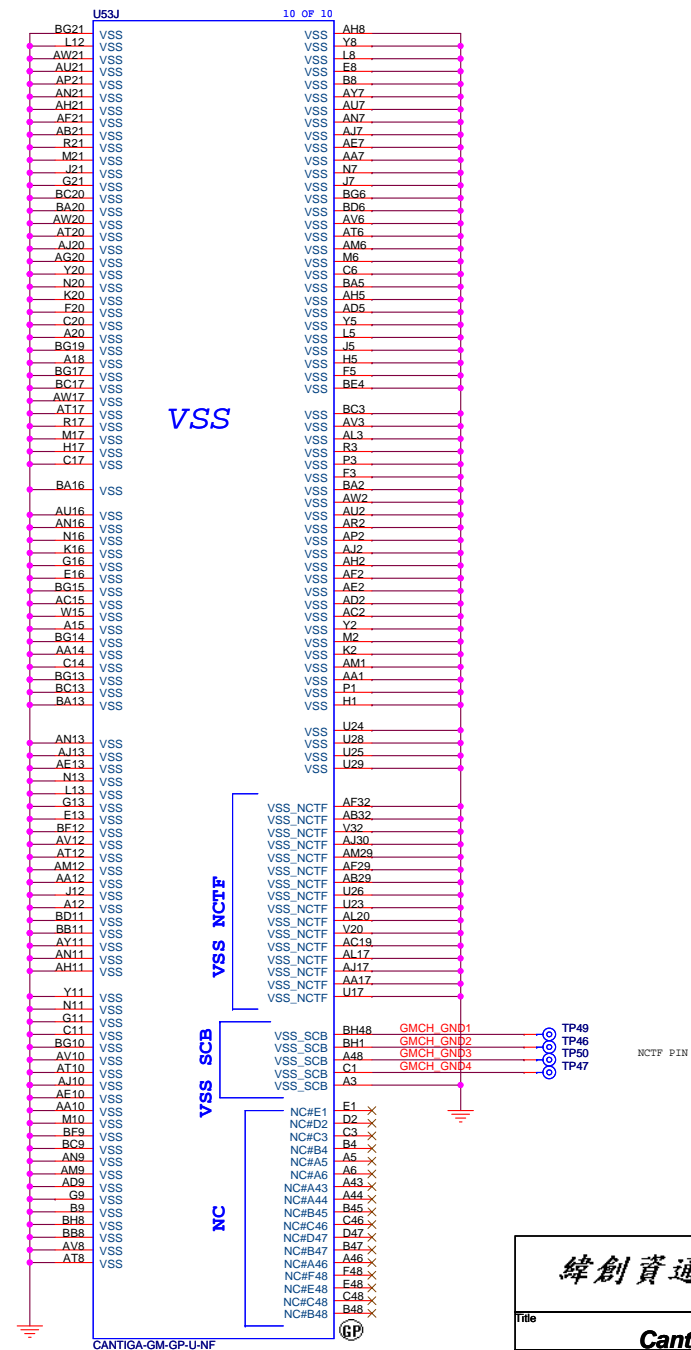
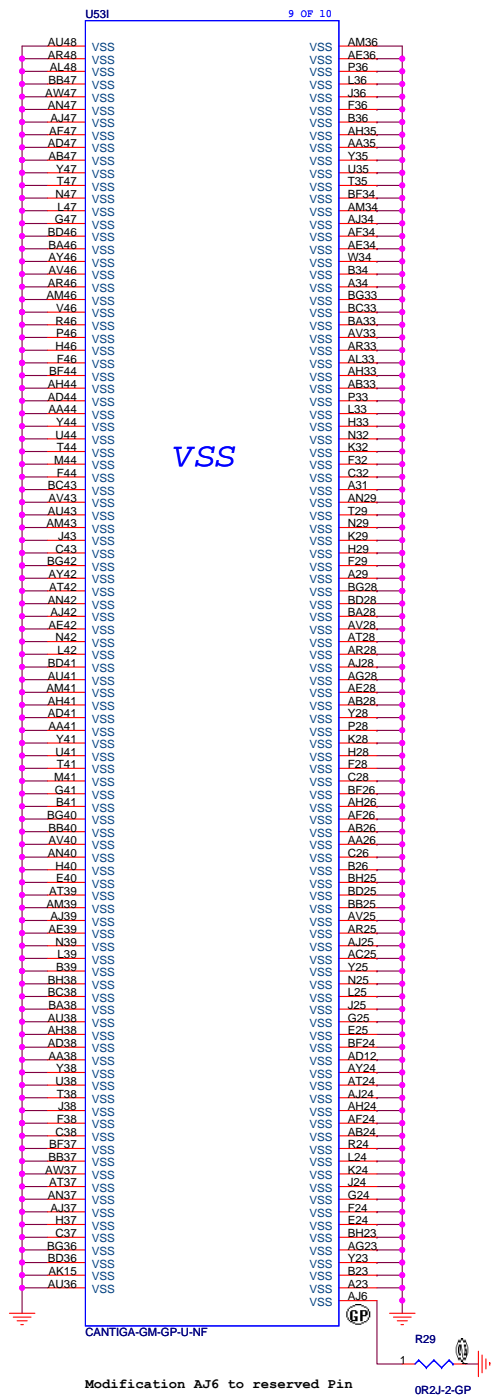
Place them near to the chip (< 0.5")




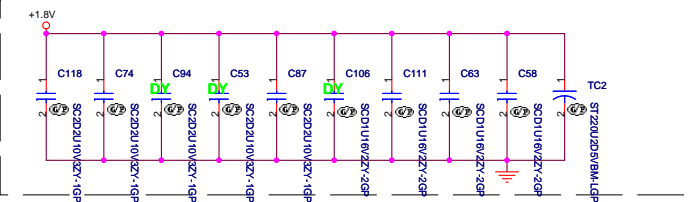
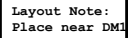
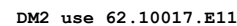
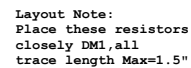






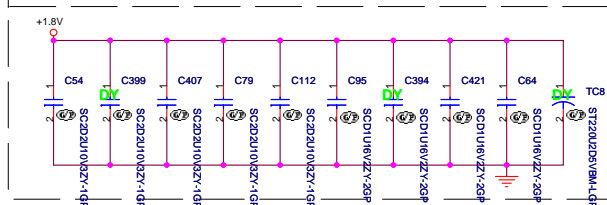


 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Mu Rd., Hsichih, Taipei Hsin 221, Taiwan, R.O.C.	
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Cantiga (6 of 6) Warrior	
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Document Number	SC
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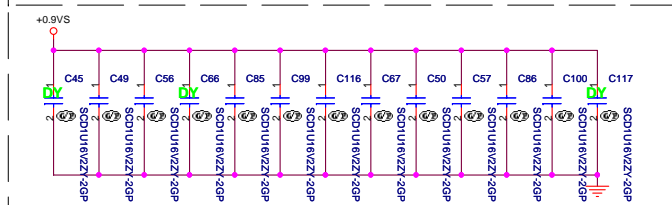
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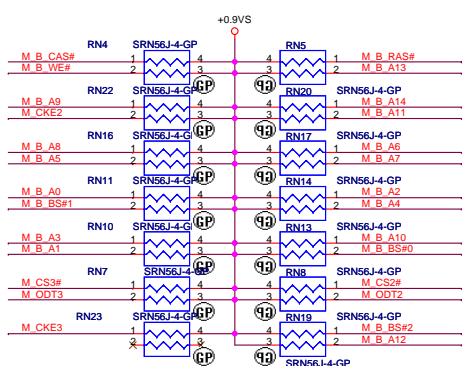
Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistors
closely DM2, all
trace length Max=1.5"



8 M_B_BS#2
8 M_B_BS#0
8 M_B_BS#1

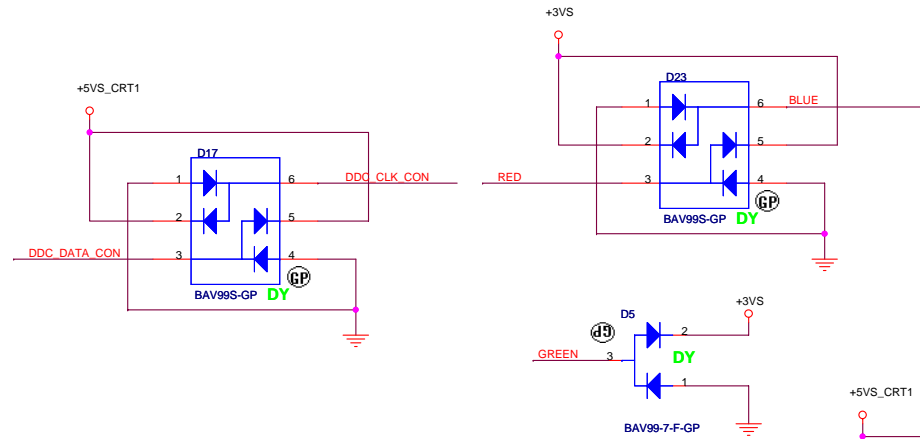
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M_B_A3	99	A3
M_B_A4	98	A4
M_B_A5	97	A5
M_B_A6	96	A6
M_B_A7	95	A7
M_B_A8	94	A8
M_B_A9	93	A9
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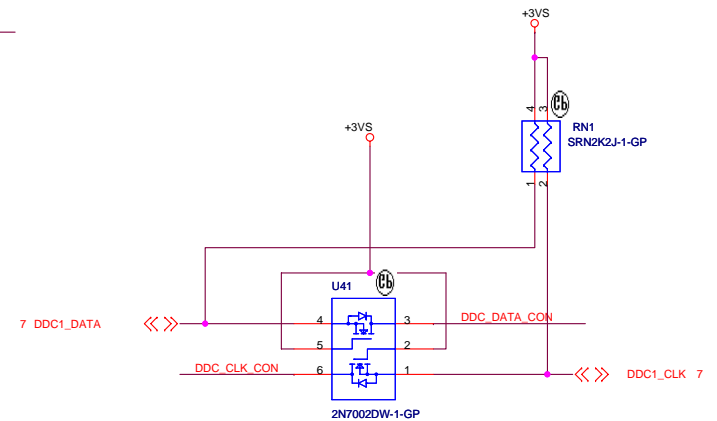
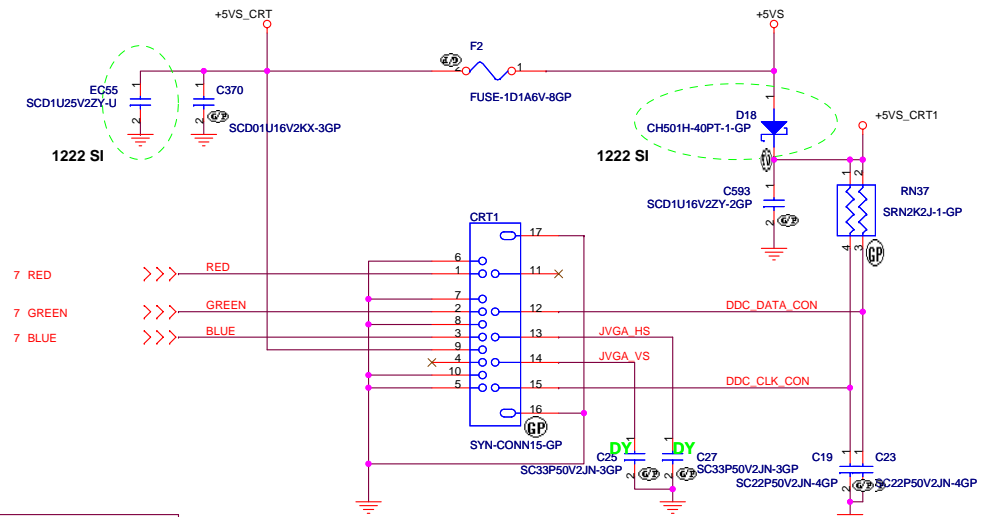
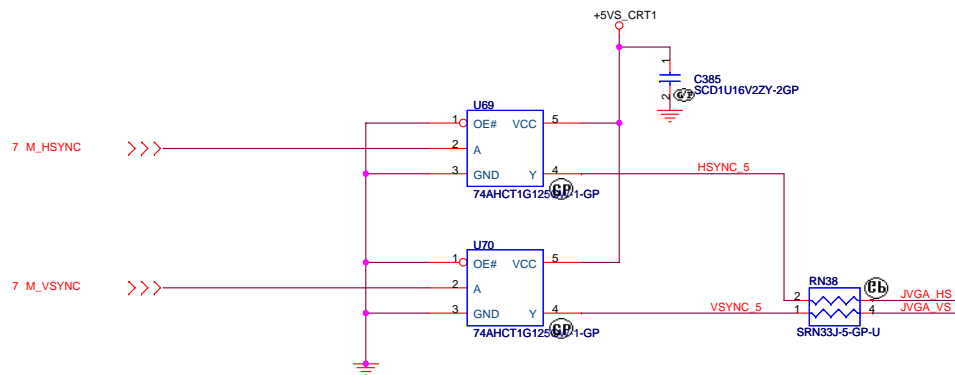
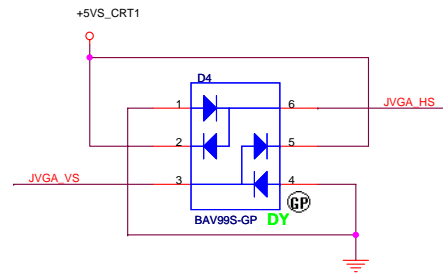
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M_B_DQ215	220	DQ215
M_B_DQ216	221	DQ216
M_B_DQ217	222	DQ217
M_B_DQ218	223	DQ218
M_B_DQ219	224	DQ219
M_B_DQ220	225	DQ220
M_B_DQ221	226	DQ221
M_B_DQ222	227	DQ222
M_B_DQ223	228	DQ223
M_B_DQ224	229	DQ224
M_B_DQ225	230	DQ225
M_B_DQ226	231	DQ226
M_B_DQ227	232	DQ227
M_B_DQ228	233	DQ228
M_B_DQ229	234	DQ229
M_B_DQ230	235	DQ230
M_B_DQ231	236	DQ231
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M_B_DQ328	333	DQ328
M_B_DQ329	334	DQ329
M_B_DQ330	335	D

CRT I/F & CONNECTOR



Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



5V @ ext. CRT side

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT Connector

Size
A3

Document Number

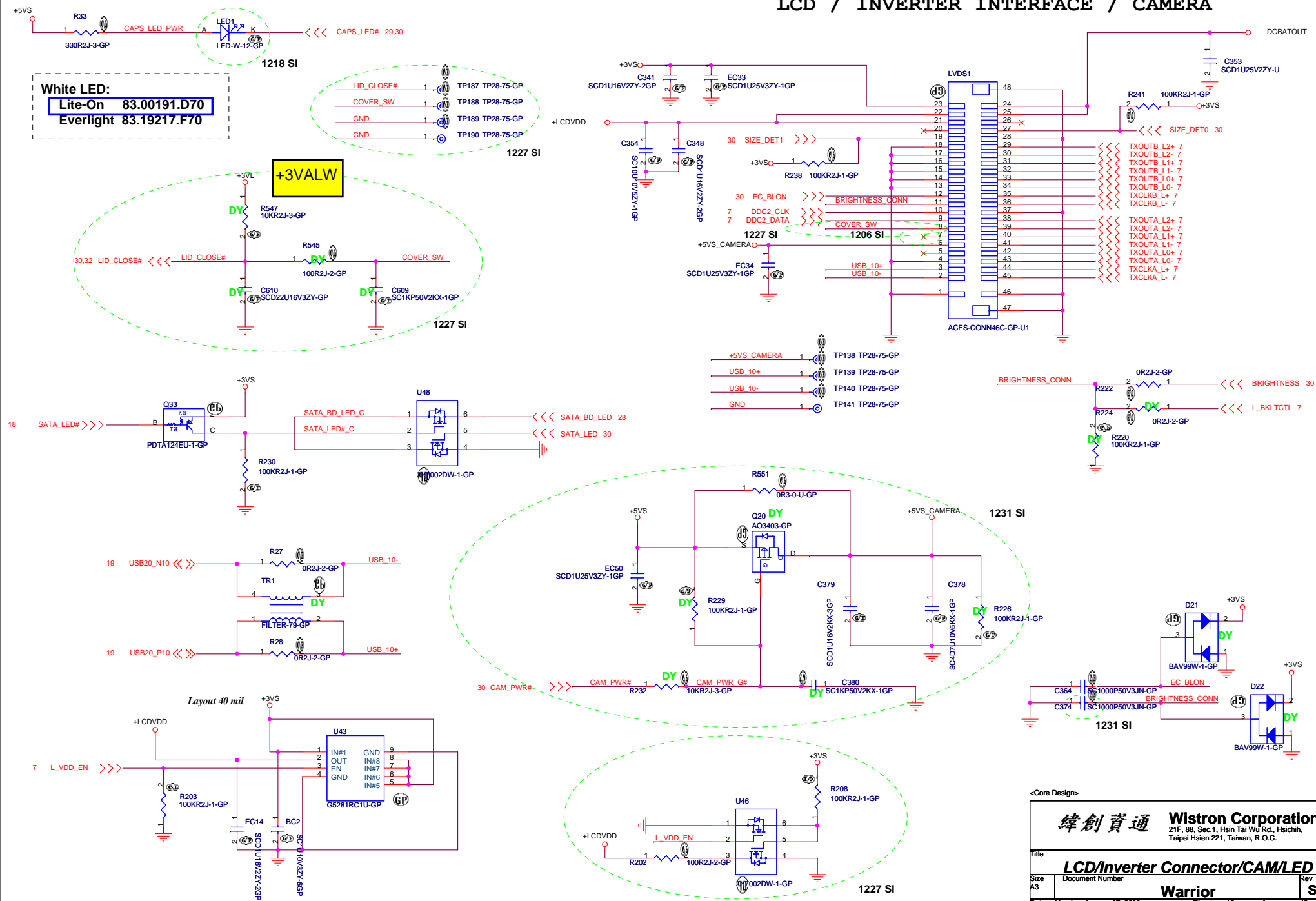
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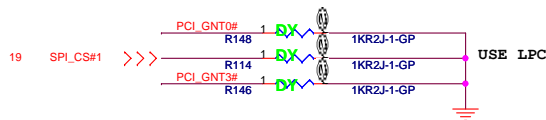
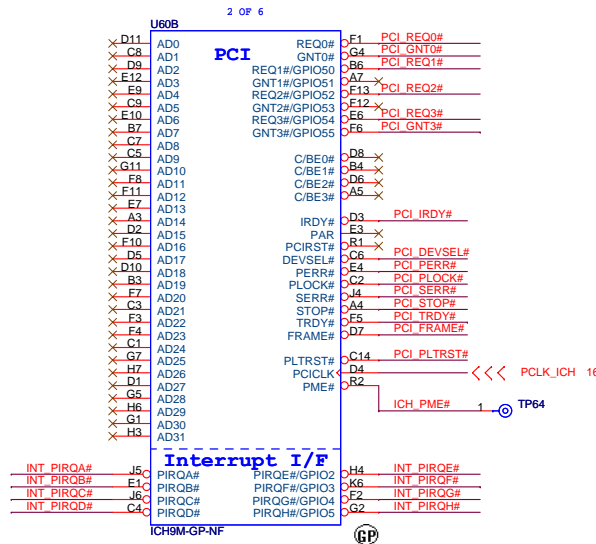
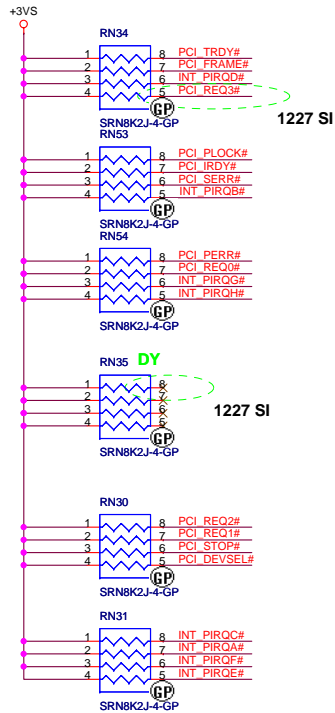
Rev
SC

Date: Monday, January 07, 2008

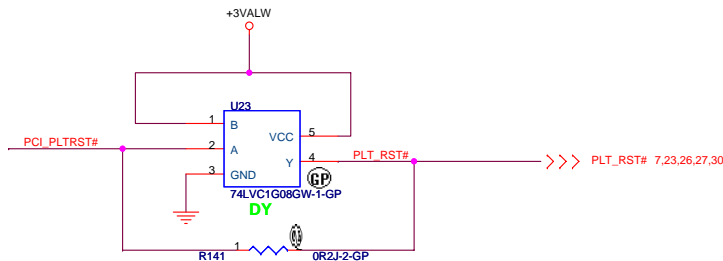
Sheet 14 of 42

LCD / INVERTER INTERFACE / CAMERA





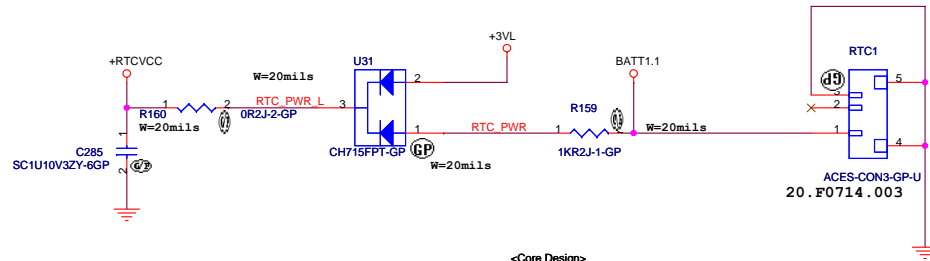
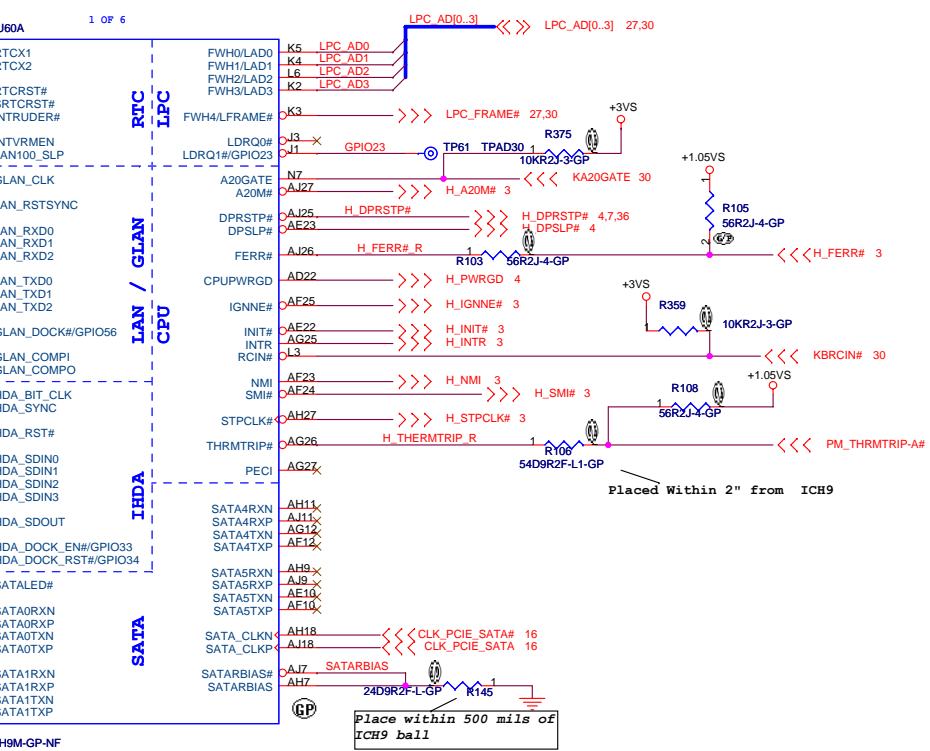
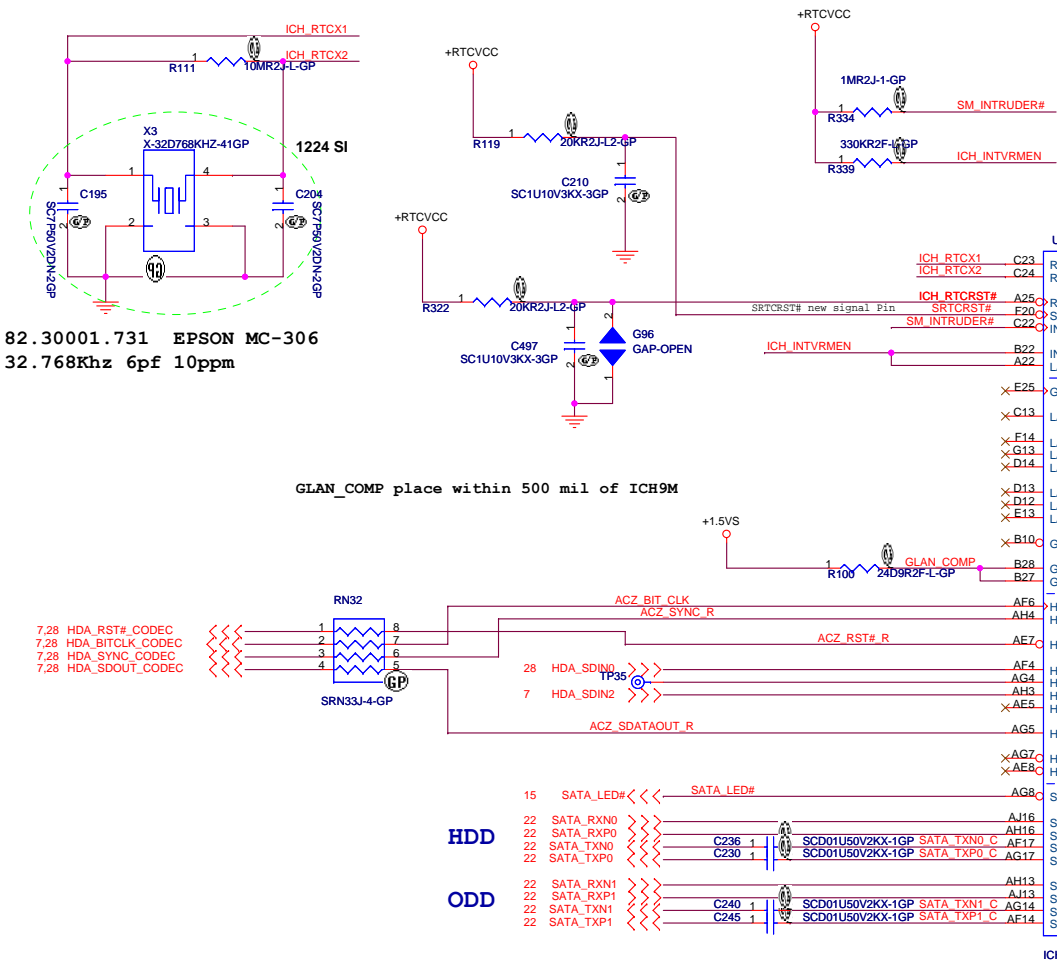
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	



<Core Design>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ICH9-M (1 of 5)			
Size	Document Number		Rev
	Warrior		SC
Date:	Monday, January 07, 2008	Sheet	17 of 42

82.30001.731 EPSON MC-306
32.768Khz 6pf 10ppm



Integrated VccSus1_05,VccSus1_5,VccCl1_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCl1_05		
LAN100_SLP	High=Enable	Low=Disable

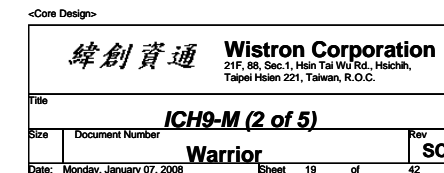
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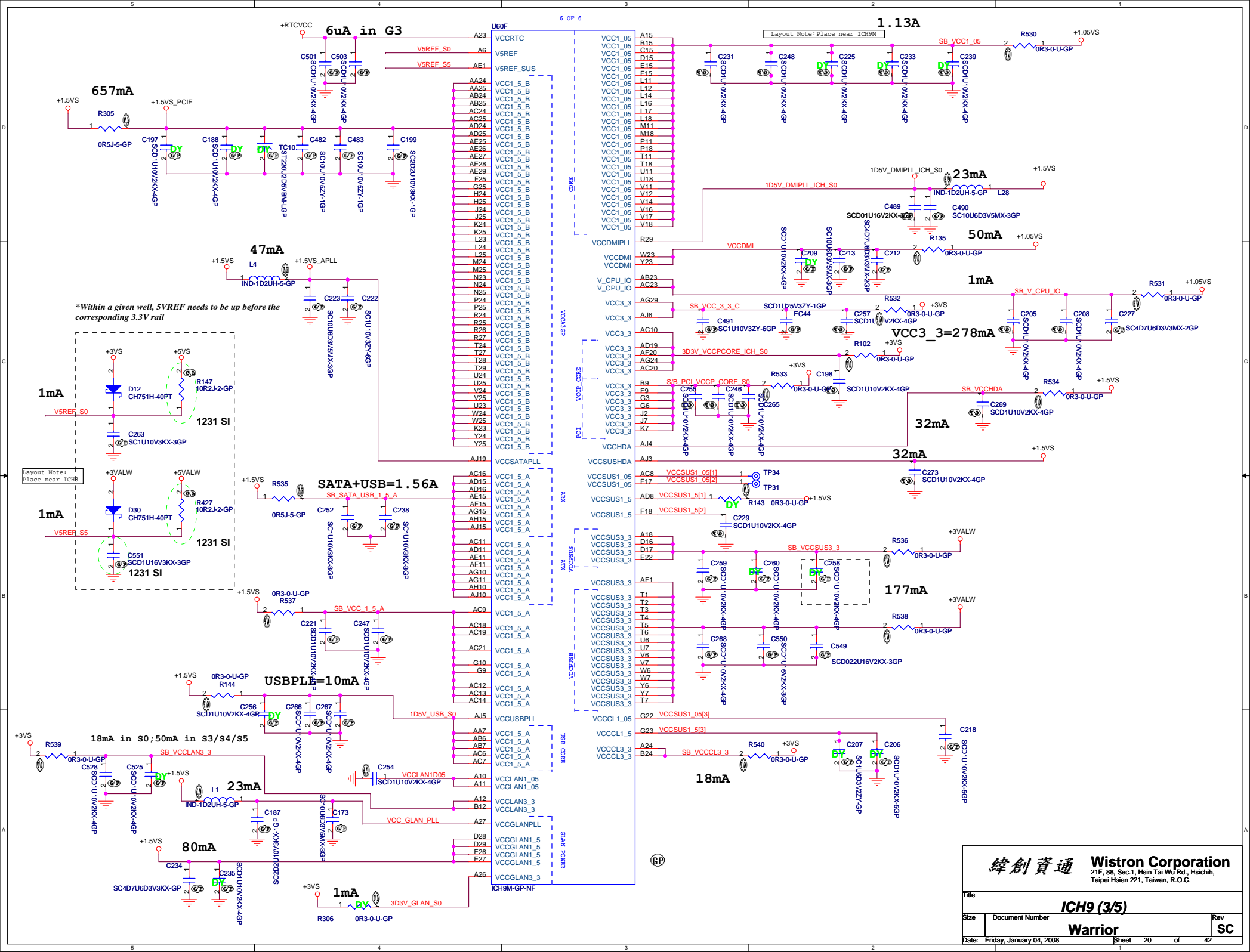
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

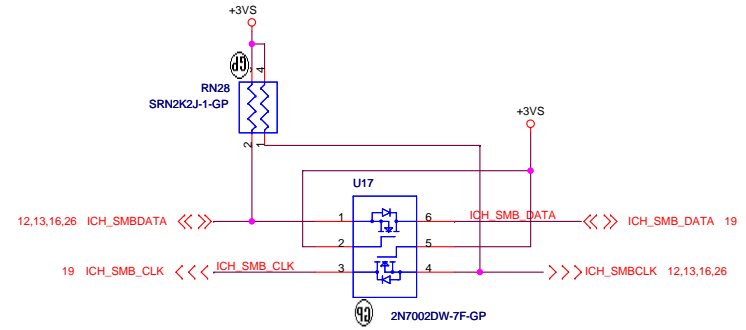
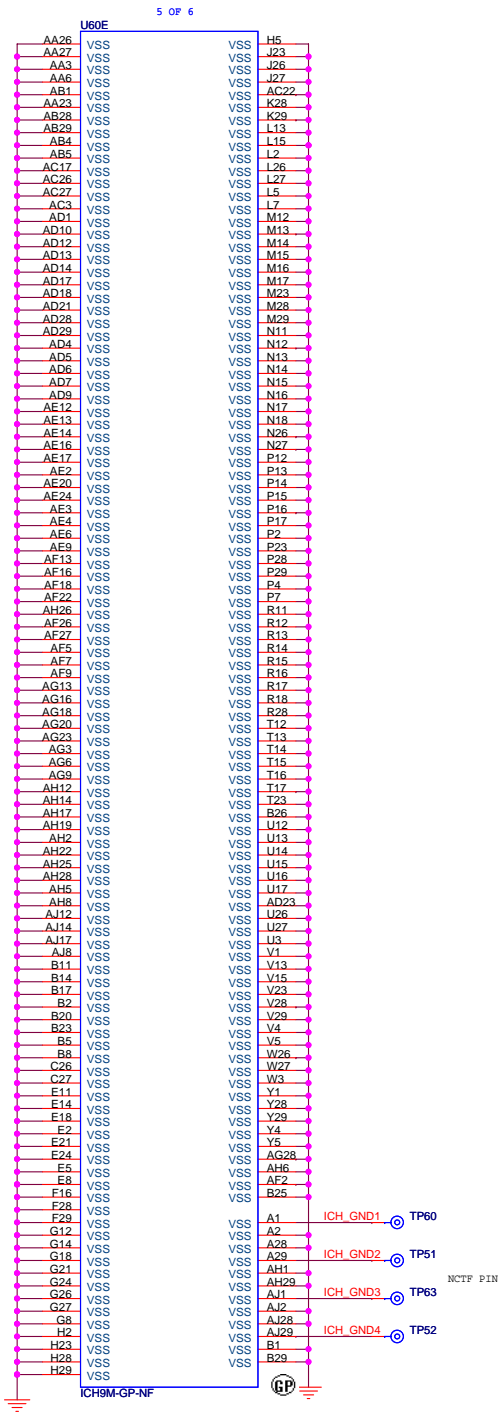
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Size: Document Number: Rev: SC

Date: Monday, January 07, 2008 Sheet: 18 of 42



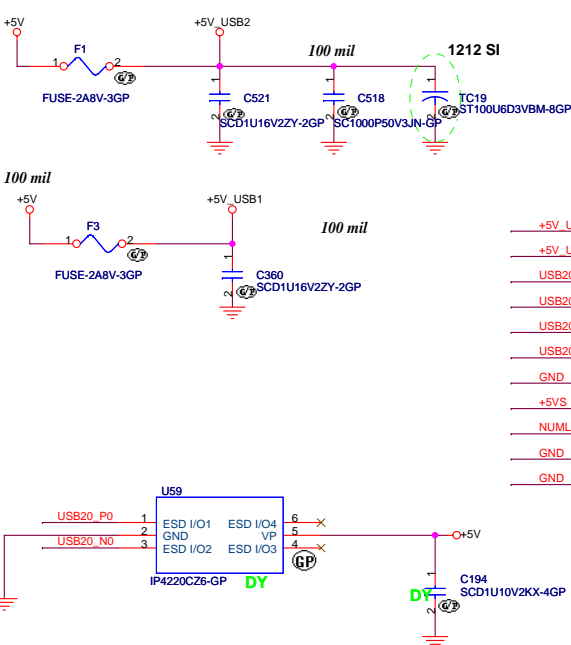




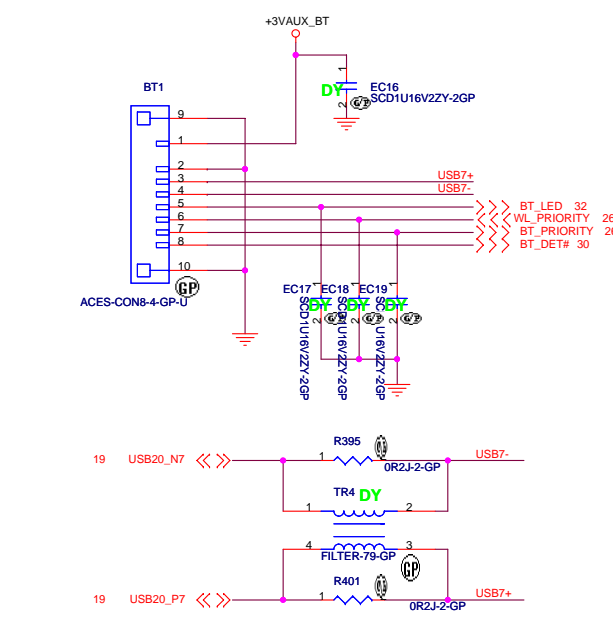
SMBUS

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title ICH9-M (4 of 4)			
Size	Document Number	Rev	SC
Date: Monday, January 07, 2008 Sheet 21 of 42			

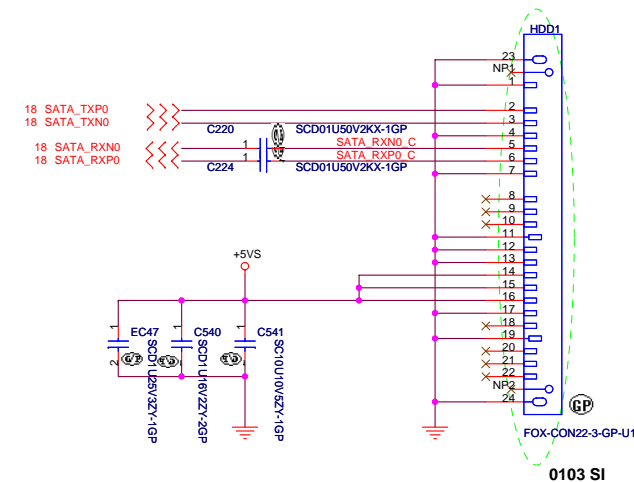
USB PORT



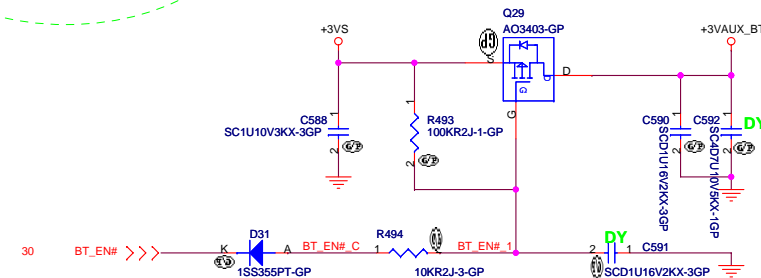
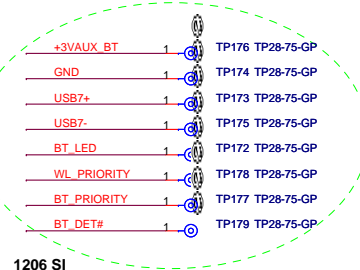
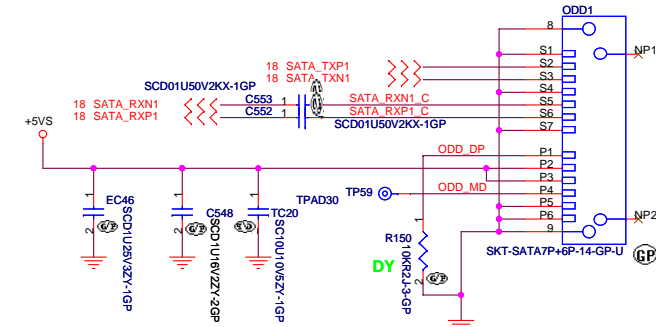
BLUETOOTH

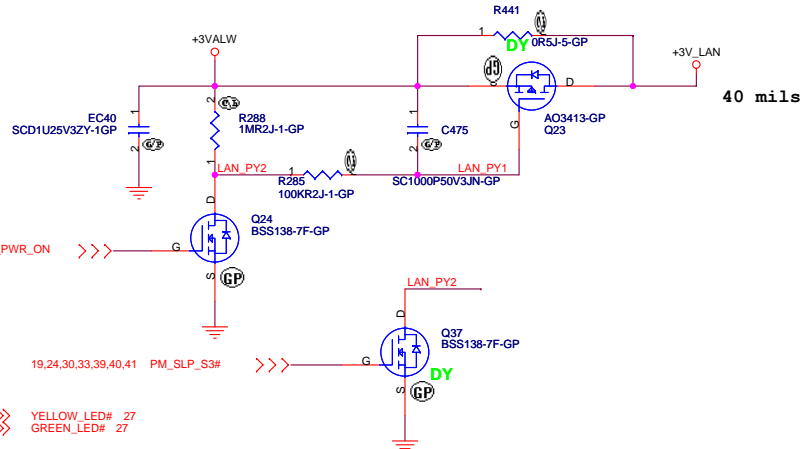
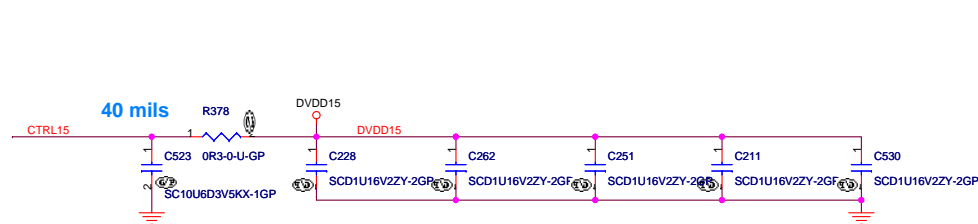
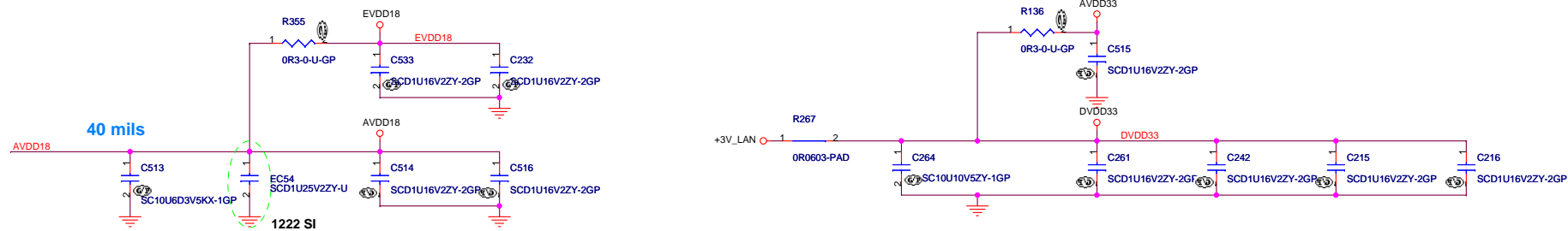


SATA HD Connector

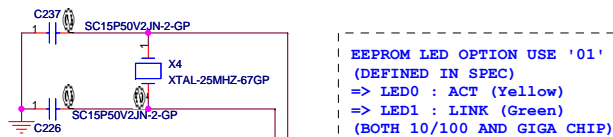


ODD Connector





R548 should be 2.49K 1% ohm for 8102E,
R548 should be 2K 1% for 8101E.

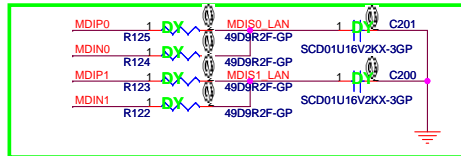


EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT (Yellow)
=> LED1 : LINK (Green)
(BOTH 10/100 AND GIGA CHIP)

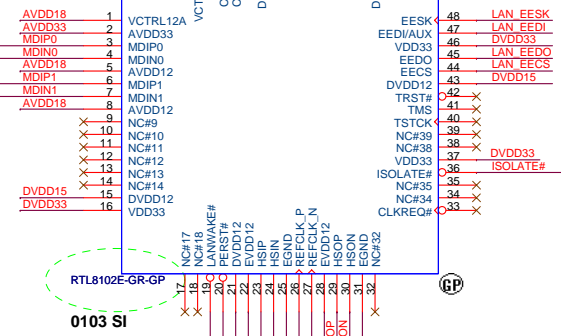
19,24,30,33,39,40,41 PM_SLP_S3#

YELLOW_LED# 27
GREEN_LED# 27

8101E use this circuit, 8102E dummy this circuit

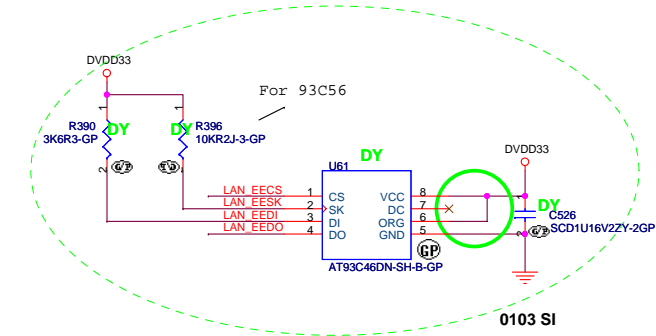


0103 SI



0103 SI

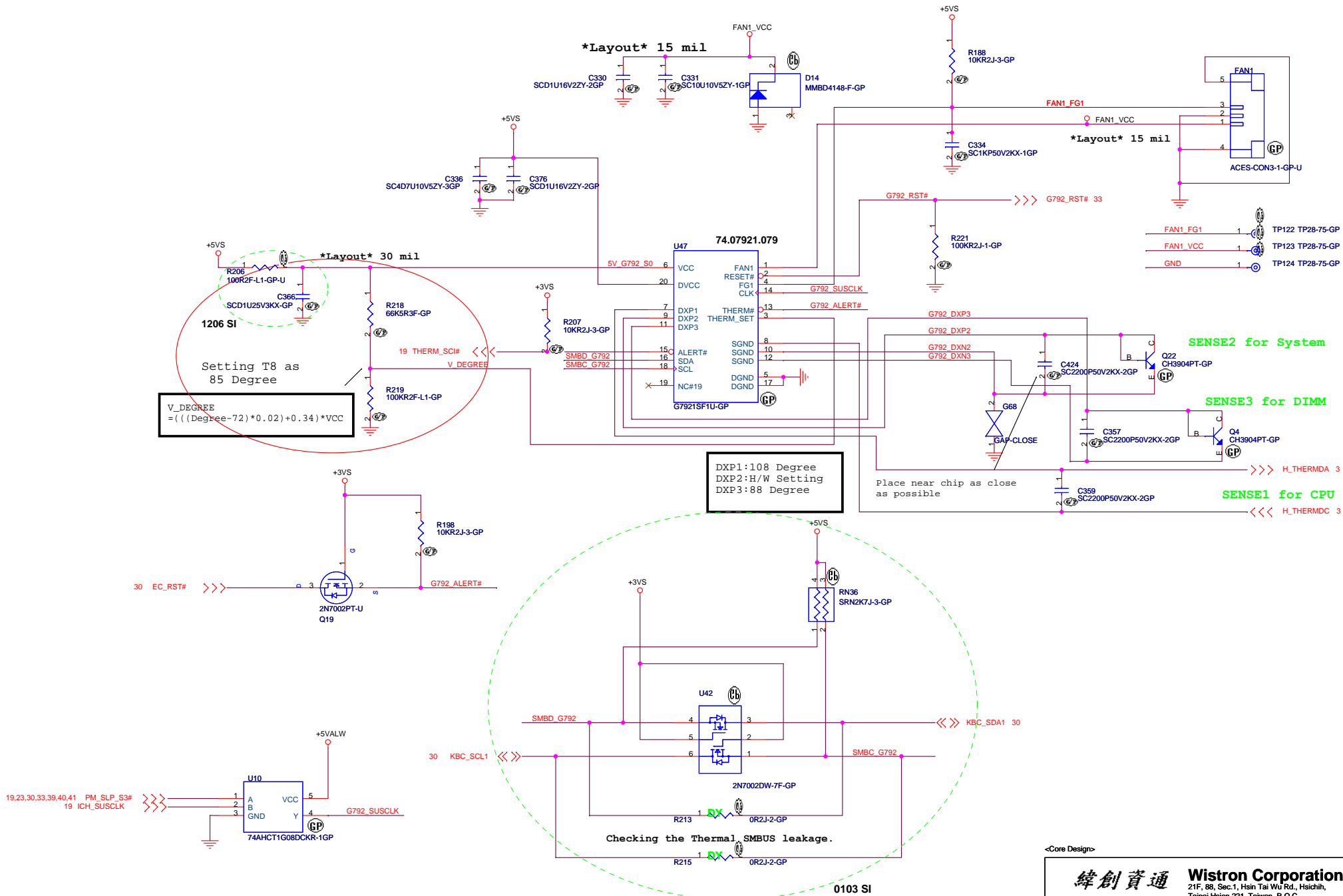
1206 SI



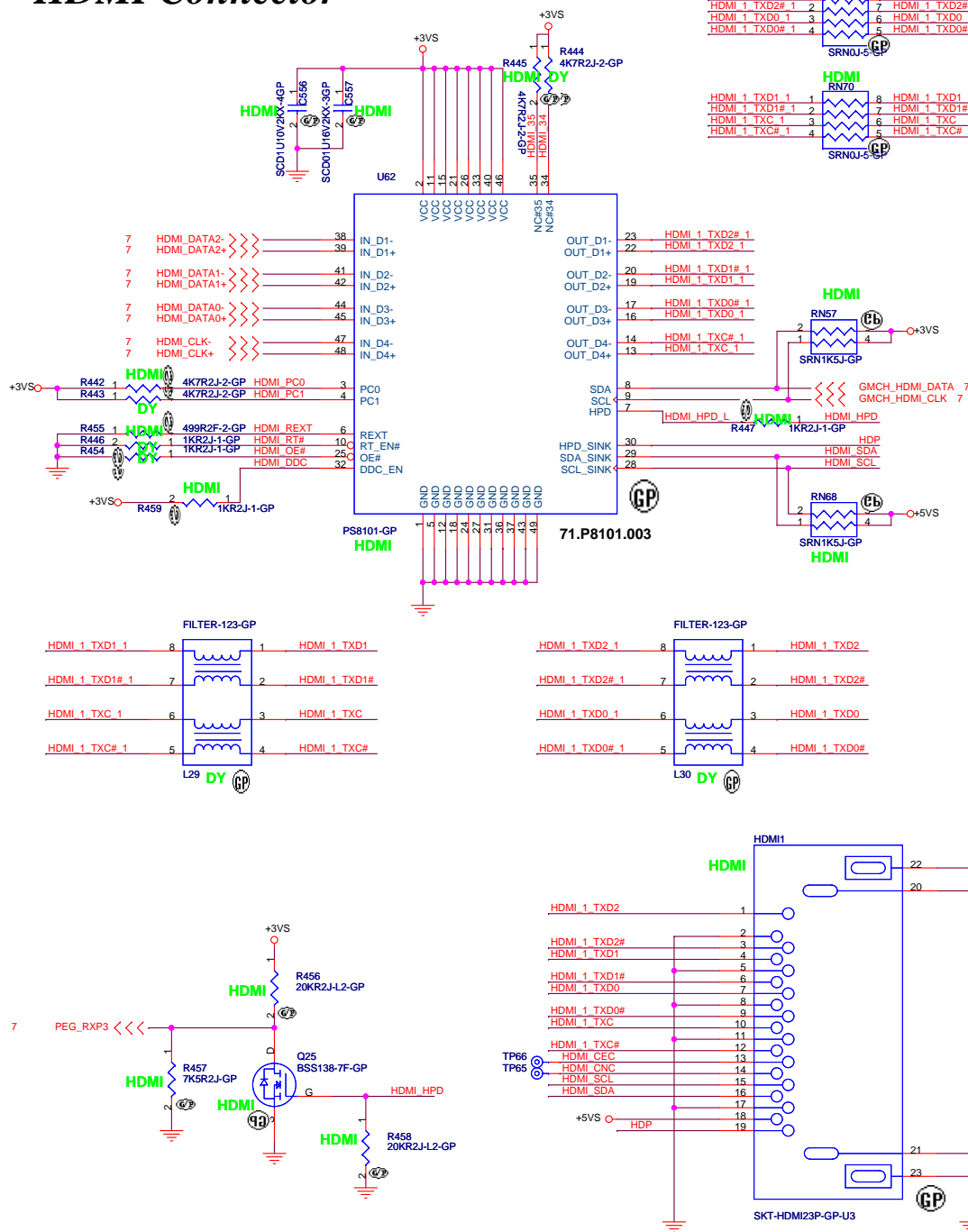
0103 SI

<Core Design>

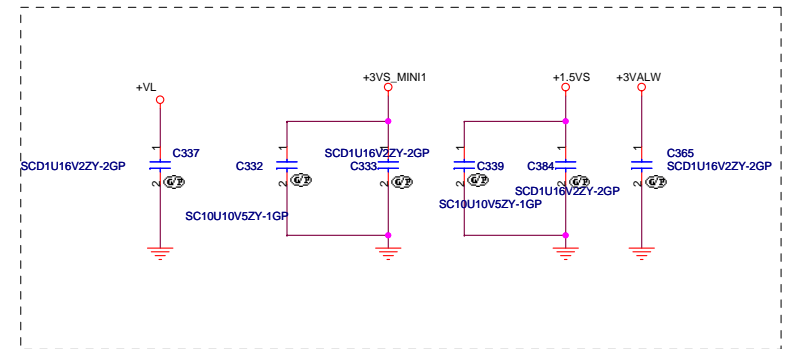
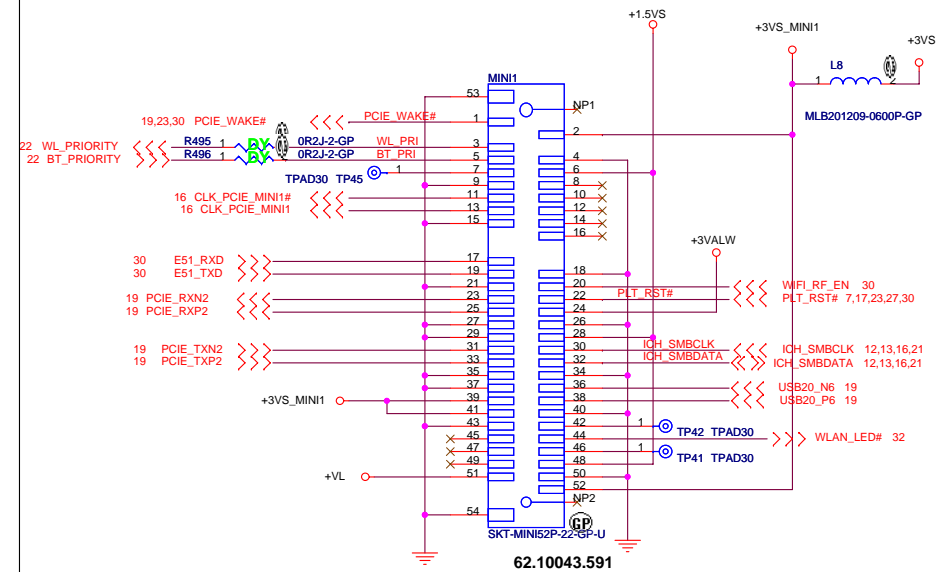
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
		RTL8101E	
Size A3	Document Number	Rev SC	
Warrior			
Date: Monday, January 07, 2008		Sheet 23 of 42	



HDMI Connector



Mini Card Connector1(802.11a/b/g)



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

100

MI

Size

Document Number

A3

— Economic Features:

Date: Monday, January 07, 2008

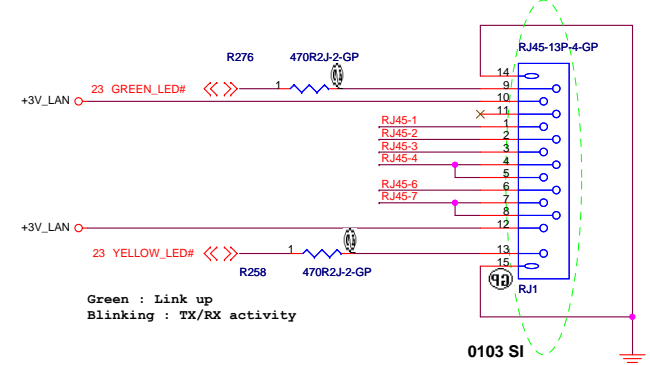
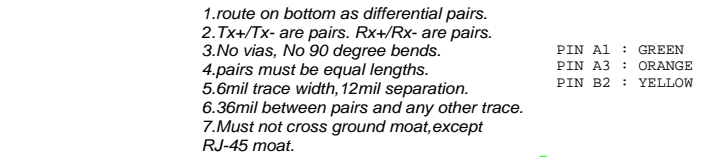
Warrior
Sheet

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Date: Monday, January 07, 2008

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E			

10/100M Lan Transformer



Remark :

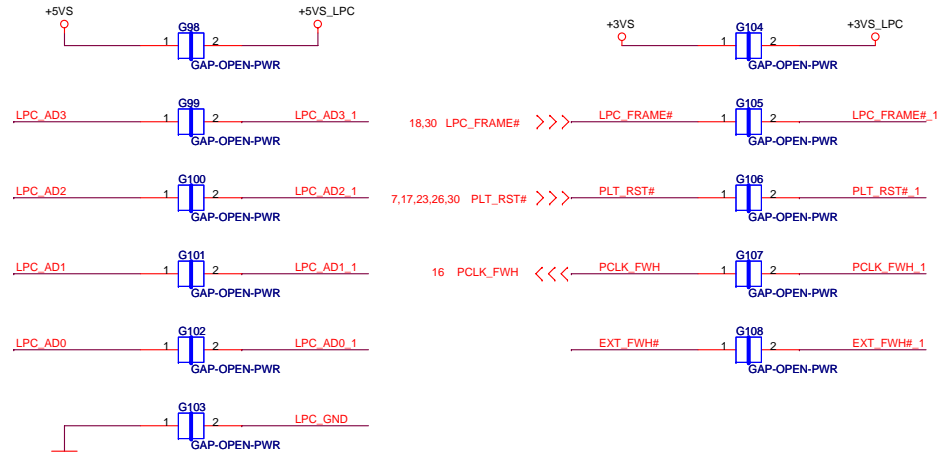
```
Add trace width to 20mils
for RJ1 pin4, 5 and pin 7, 8.
```

TOP VIEW (A)



Pin connection diagram for the FOX-GF30 module. The diagram shows a central blue box labeled 'FOX-GF30' with pins A1 through A15 on the left and B1 through B15 on the right. On the left side, there are three power supply pins: +5VS_LPC (top), +3VS_LPC (bottom), and a ground pin (middle). On the right side, there are three power supply pins: +5VS_LPC (top), +3VS_LPC (bottom), and a ground pin (middle). The diagram also shows various signal pins: PLT_RST#_1, LPC_FRAME#_1, LPC_GND, PCLK_FWH_1, LPC_AD3_1, LPC_AD2_1, LPC_AD1_1, LPC_AD0_1, EXT_FWH#_1, and their counterparts on the right. The diagram is labeled 'DEBUG1' at the top and 'FOX-GF30' at the bottom.

Please put near board edge.



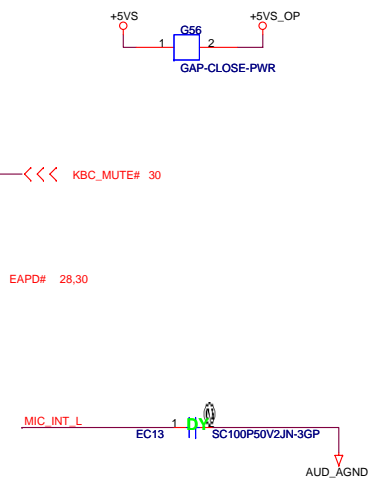
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

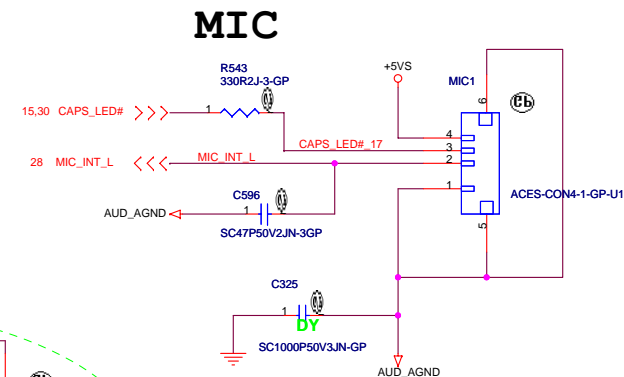
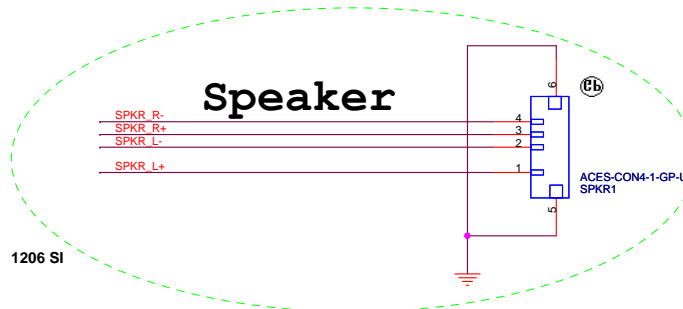
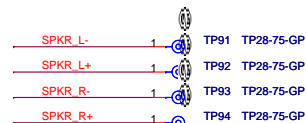
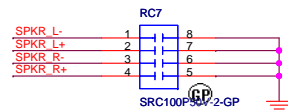
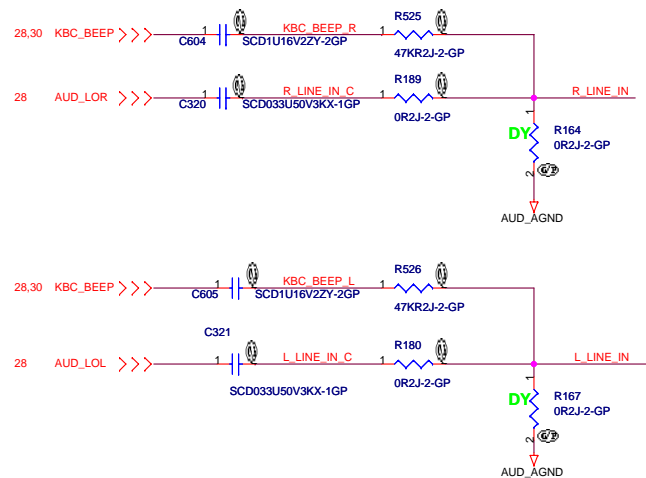
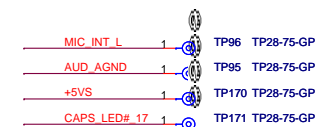
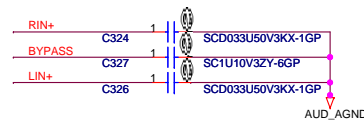
LAN CONN/Debug

Warrior

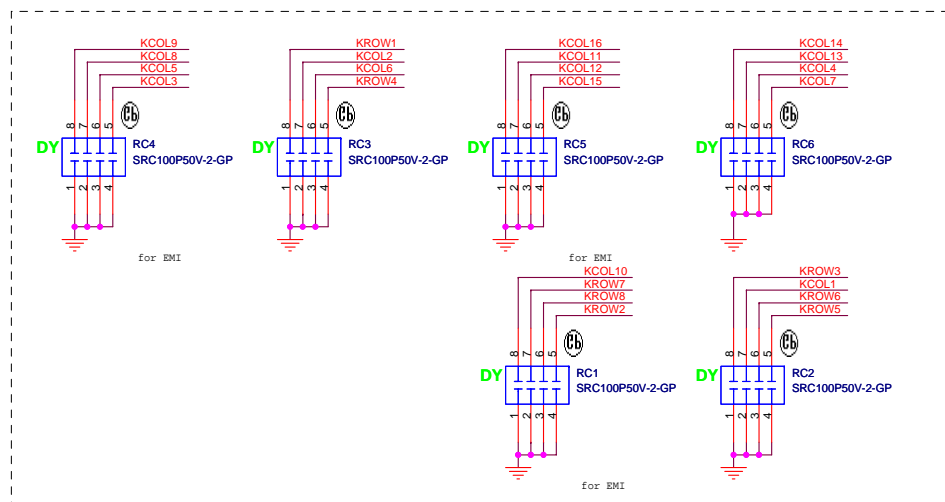
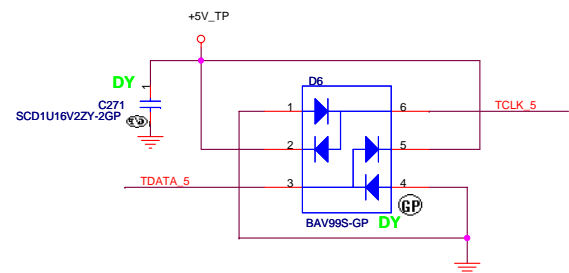
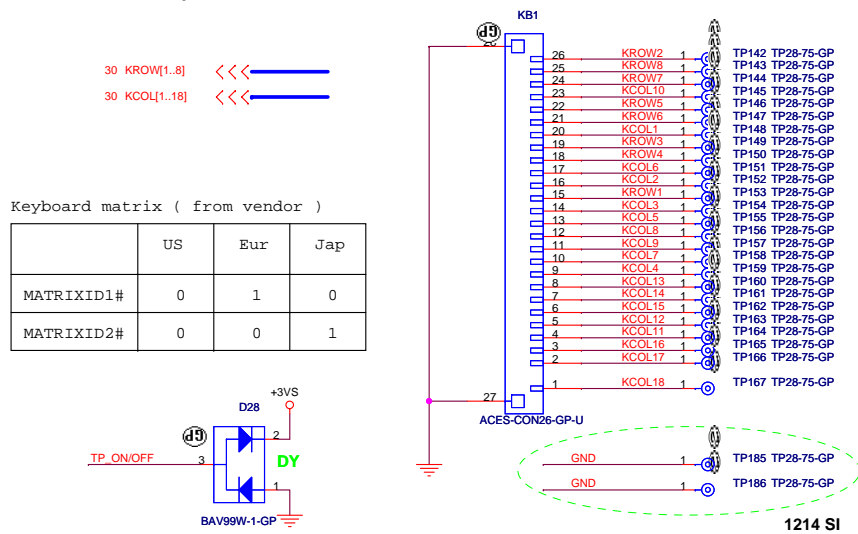
Sheet 27 of 42



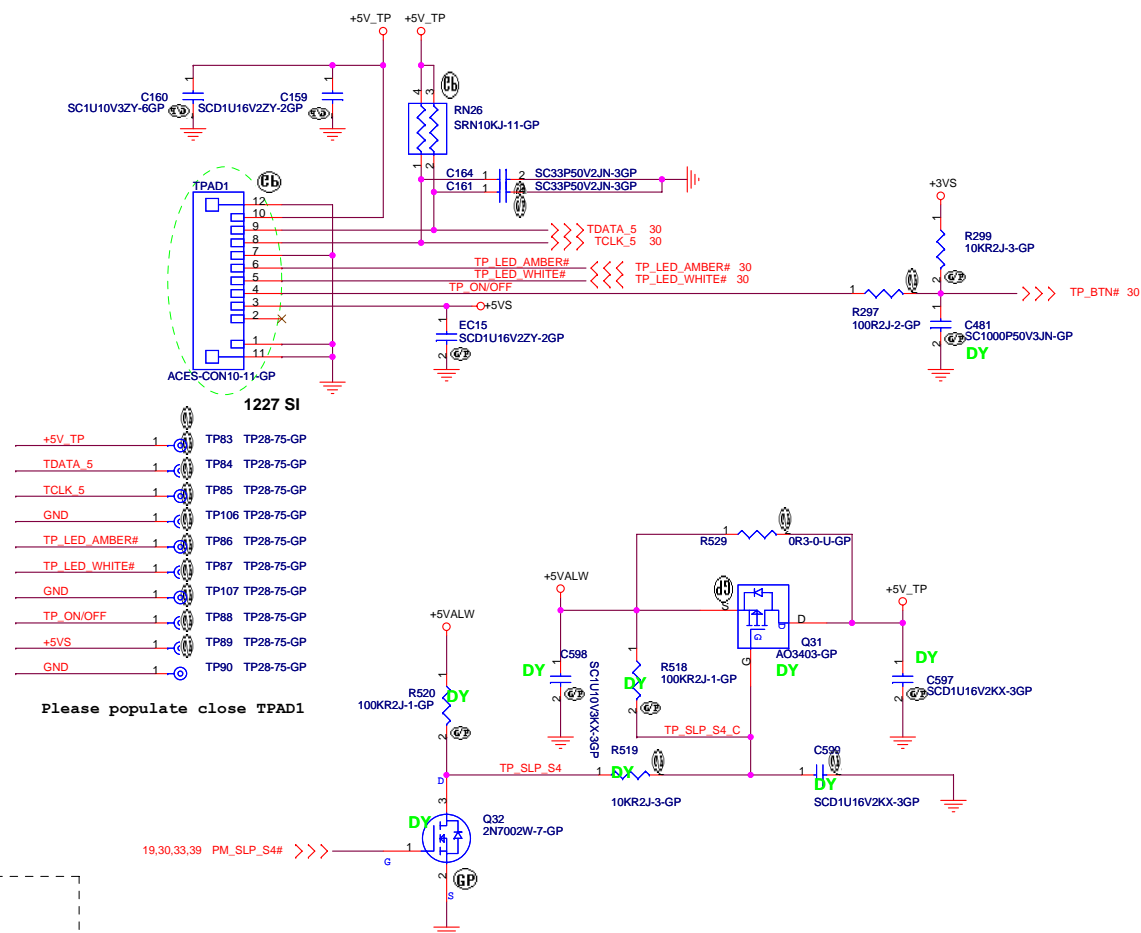
GAIN0	GAIN1	Av (dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6

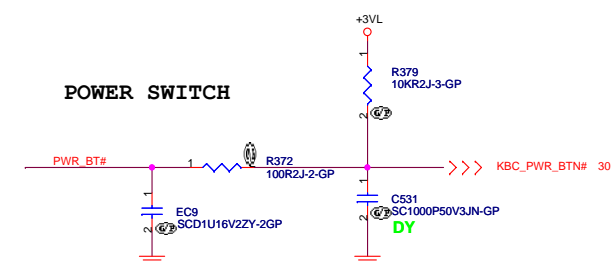
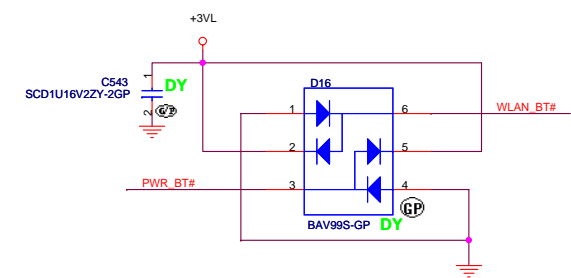
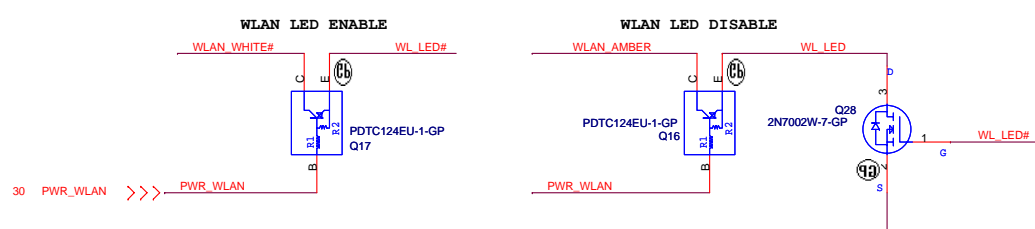
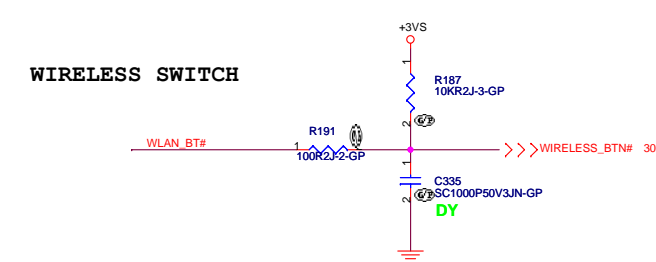
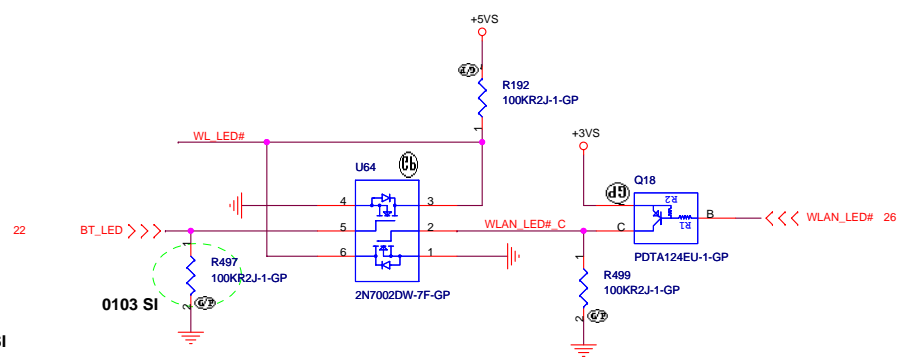
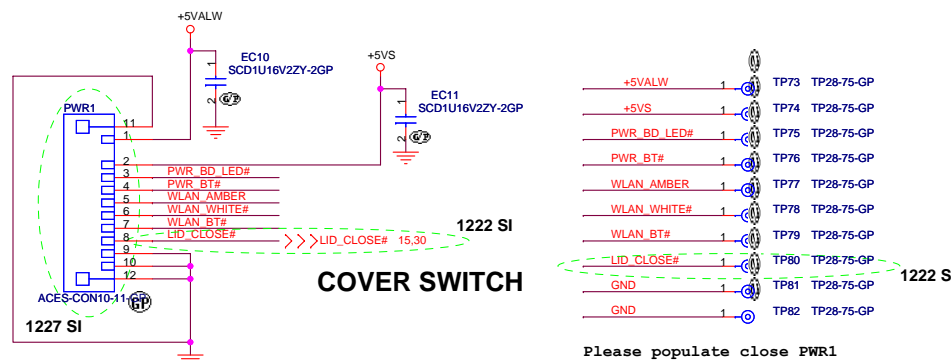
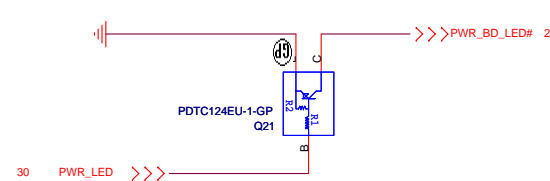
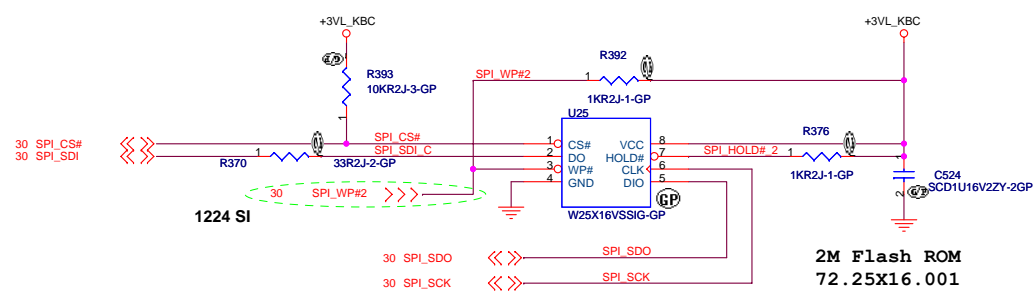


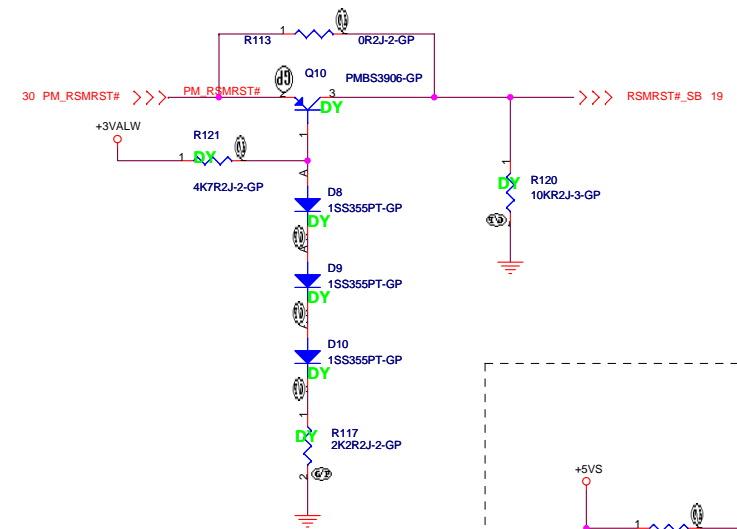
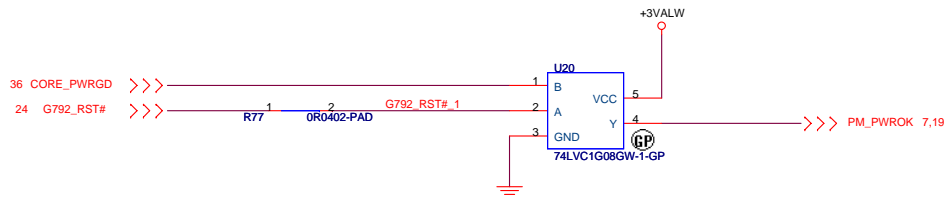
Internal KeyBoard Connector



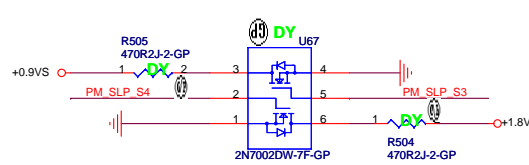
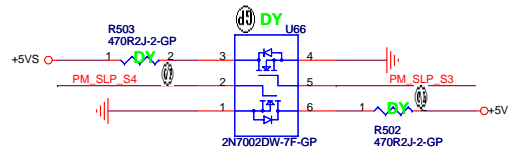
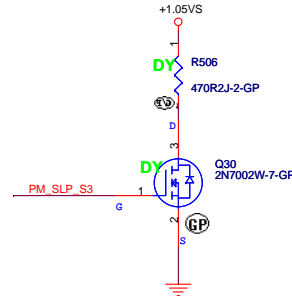
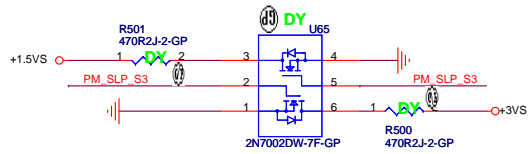
TouchPad Connector







Discharge Circuit

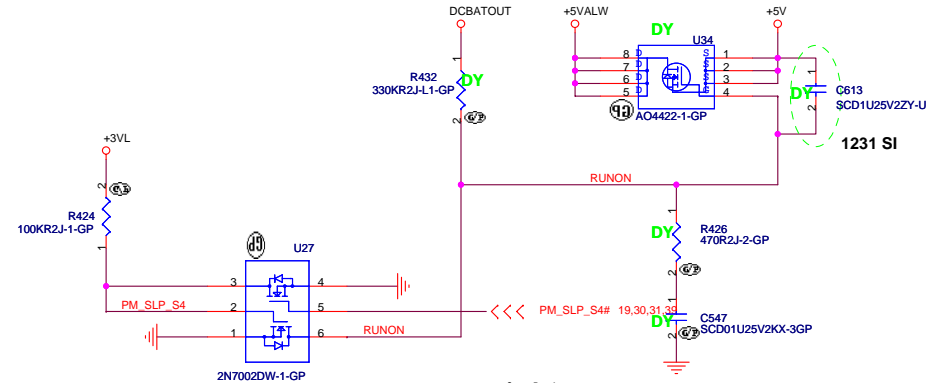
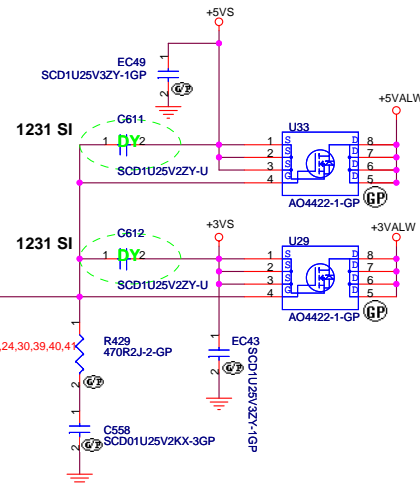
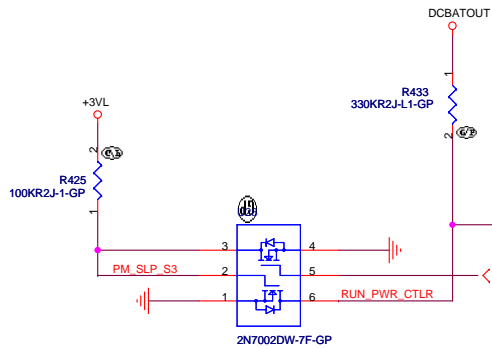


Populate close U34

+5VALW to +5VS Transfer
+3VALW to +3VS Transfer

+5VALW to +5V Transfer

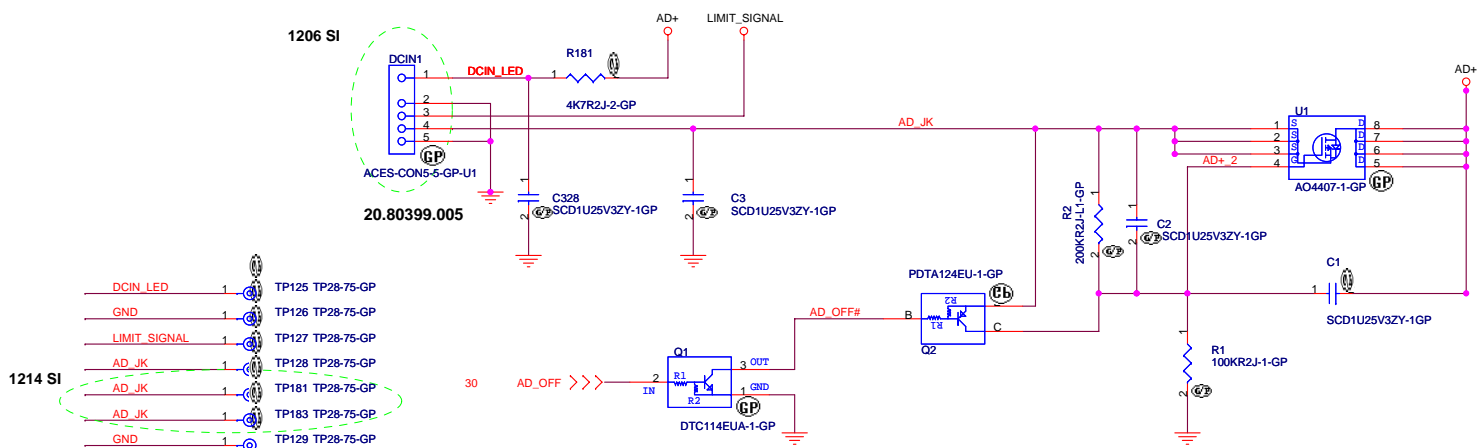
Run Power



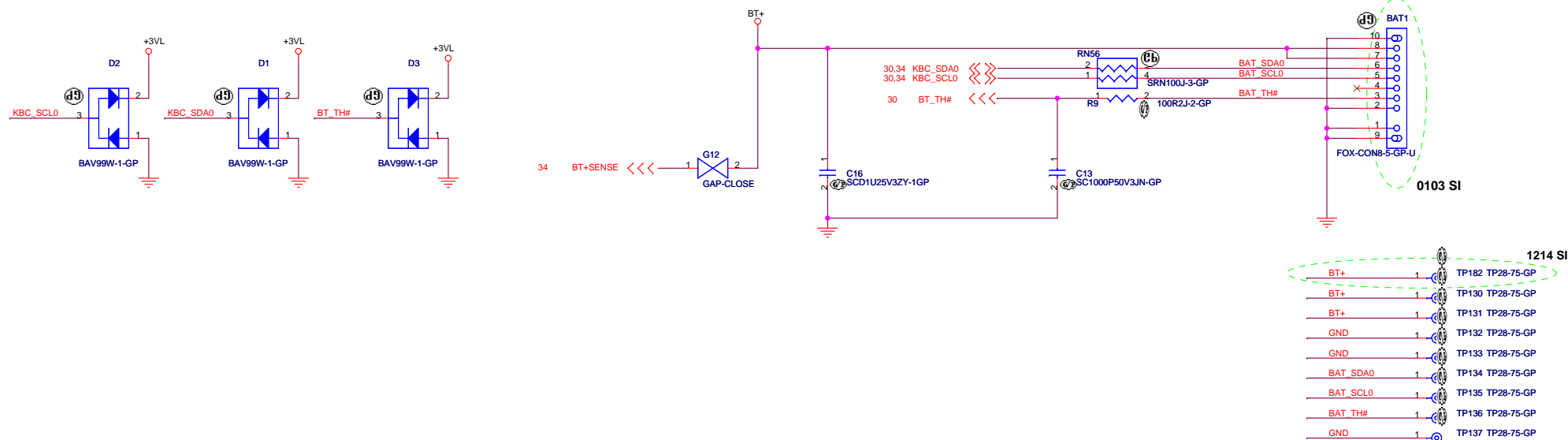
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Title	PWRPLANE	
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Adaptor in to generate DCBATOUT



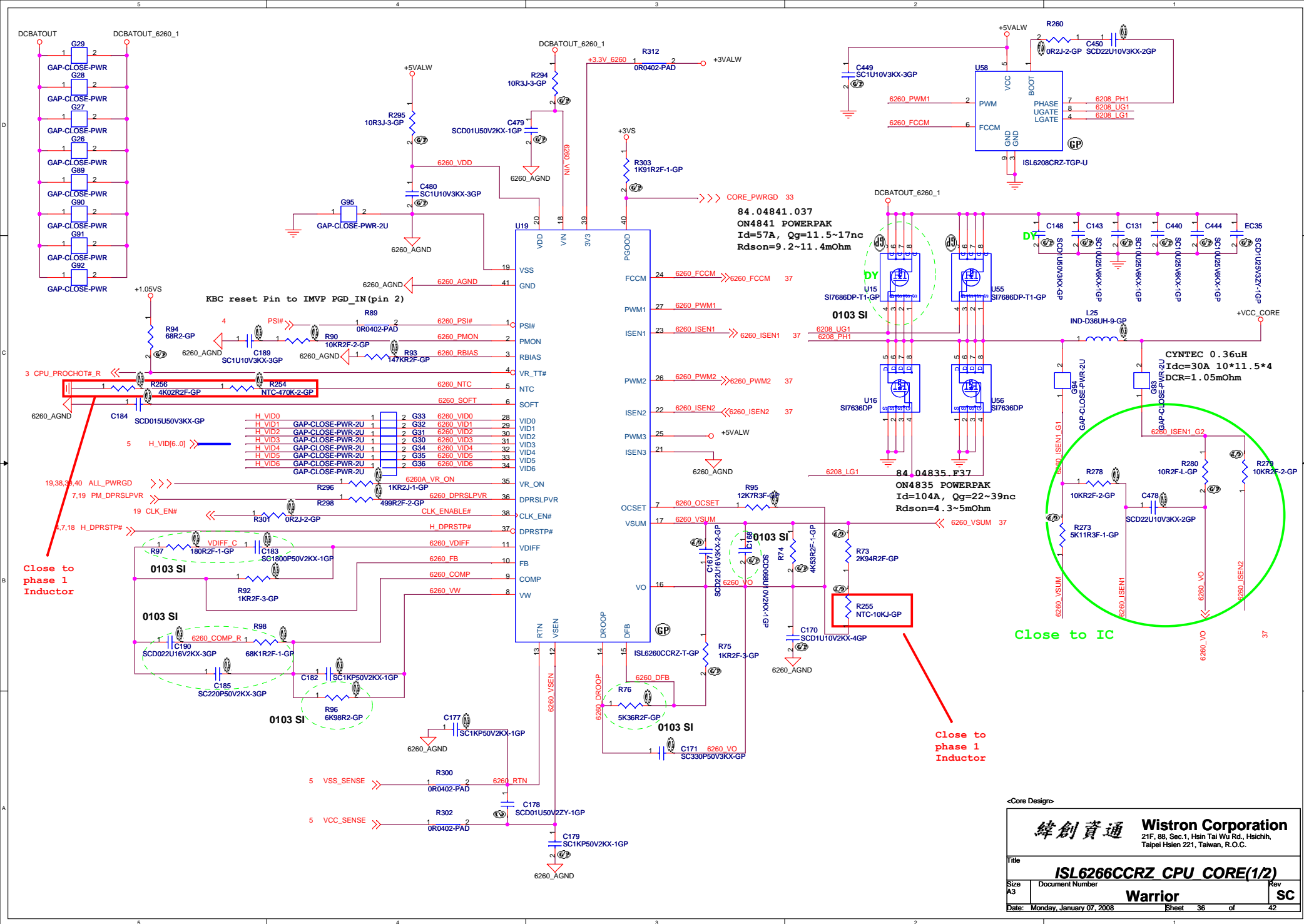
BATTERY CONNECTOR

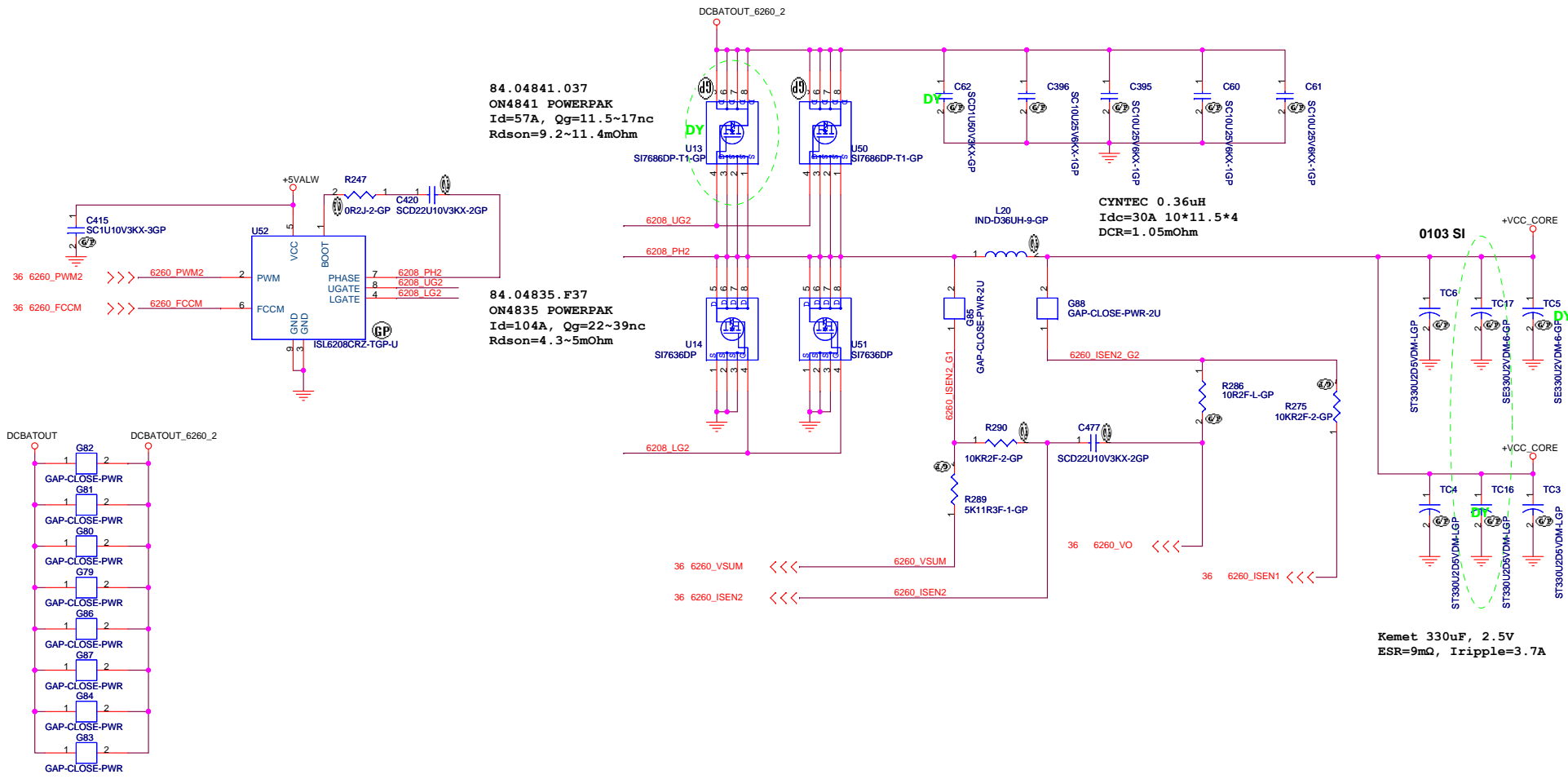


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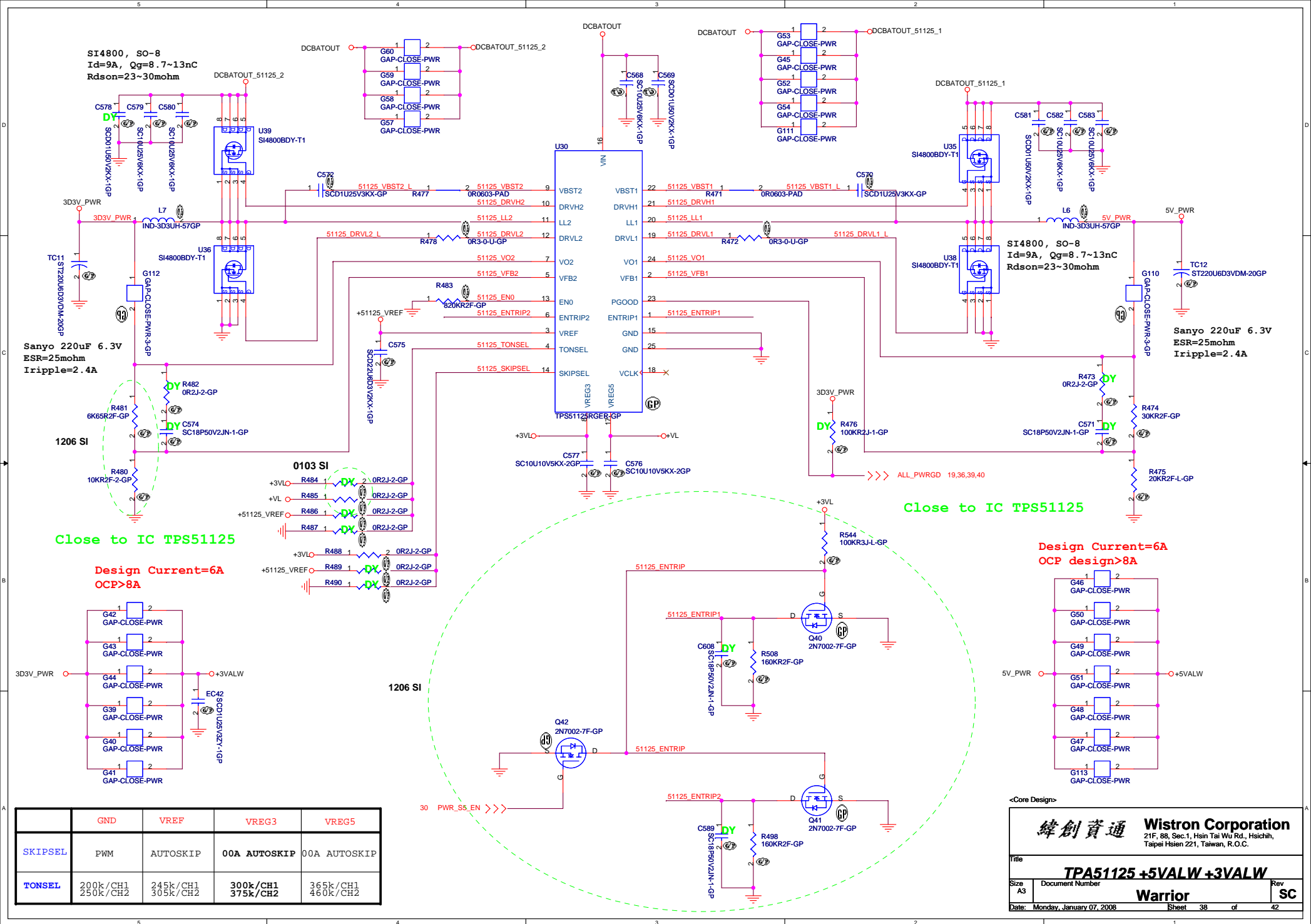
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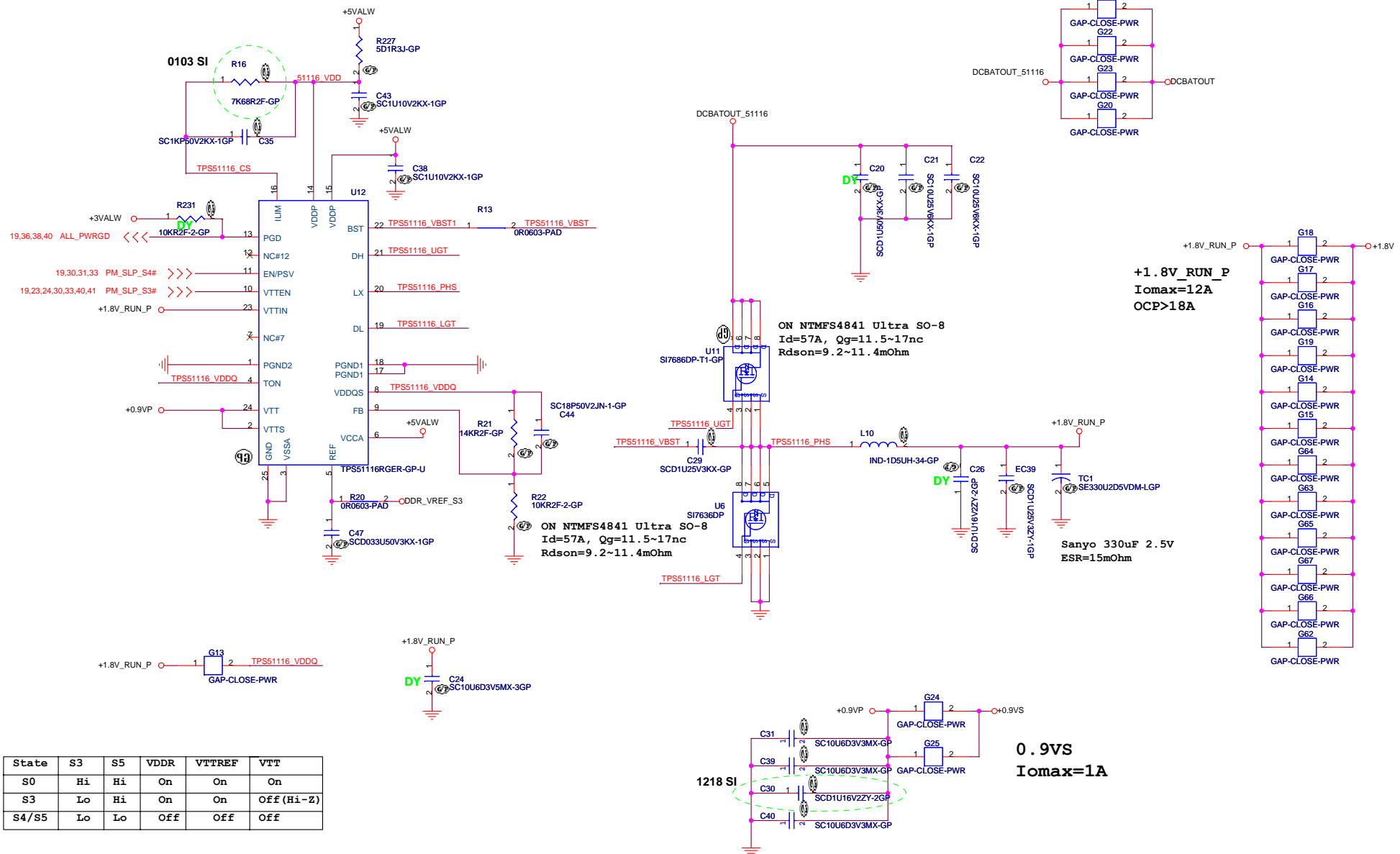


Kemet 330uF, 2.5V
ESR=9mΩ, Irripple=3.7A



	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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TPS51116 1D8V/0D9V

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Document Number

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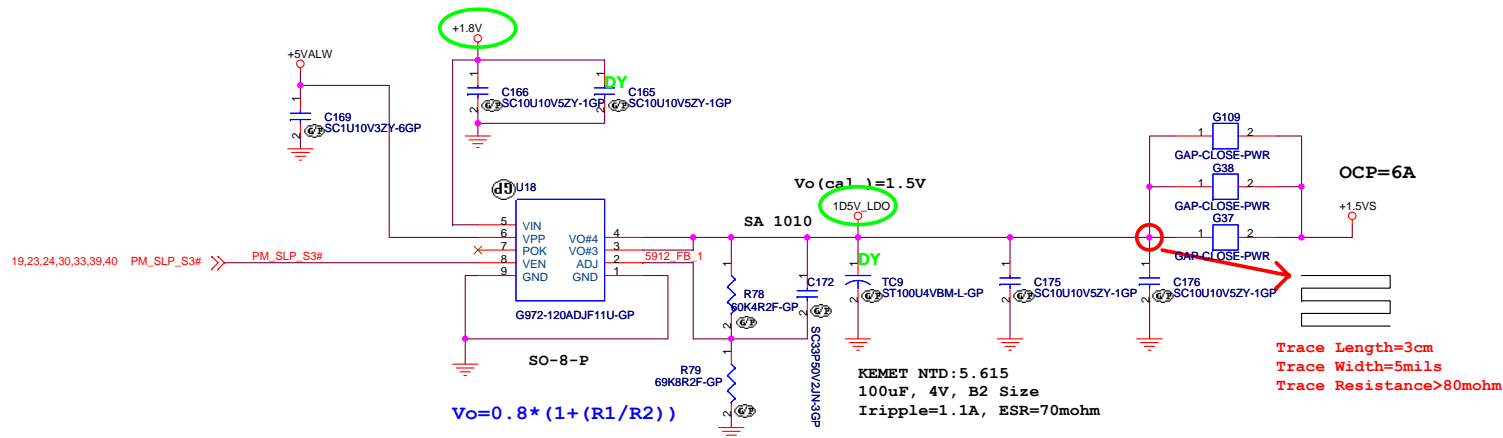
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GMT 1D5V LDO

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A3

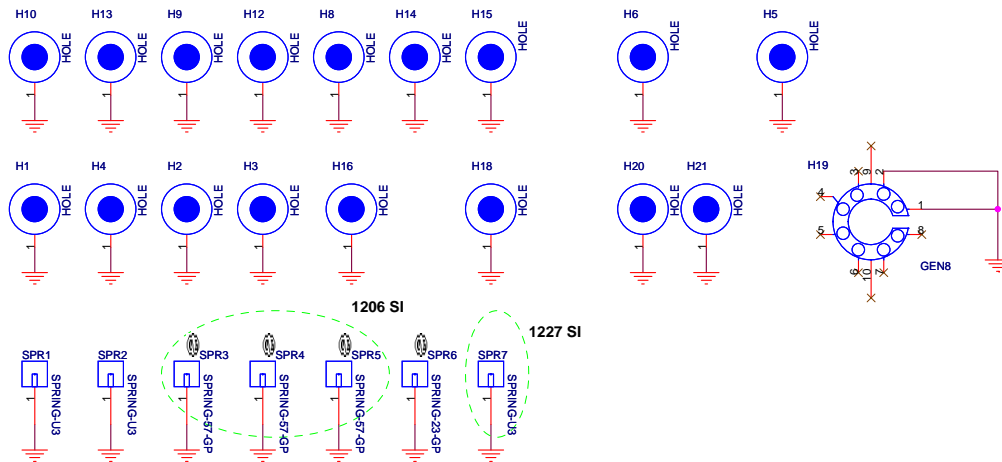
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Rev
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SPR1-2: 34.40U07.001
 SPR3-5: 34.42T14.002
 SPR6 : 34.39S07.003
 SPR7 : 34.40U07.001

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